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PRODUCTION MEASUREMENT OF FUZE COMPONENTS UNDER DYNAMIC STRESS.(U)
SEP 76 A J EISENBERGER, P KASZERMAN DAAB07-76-C-0032
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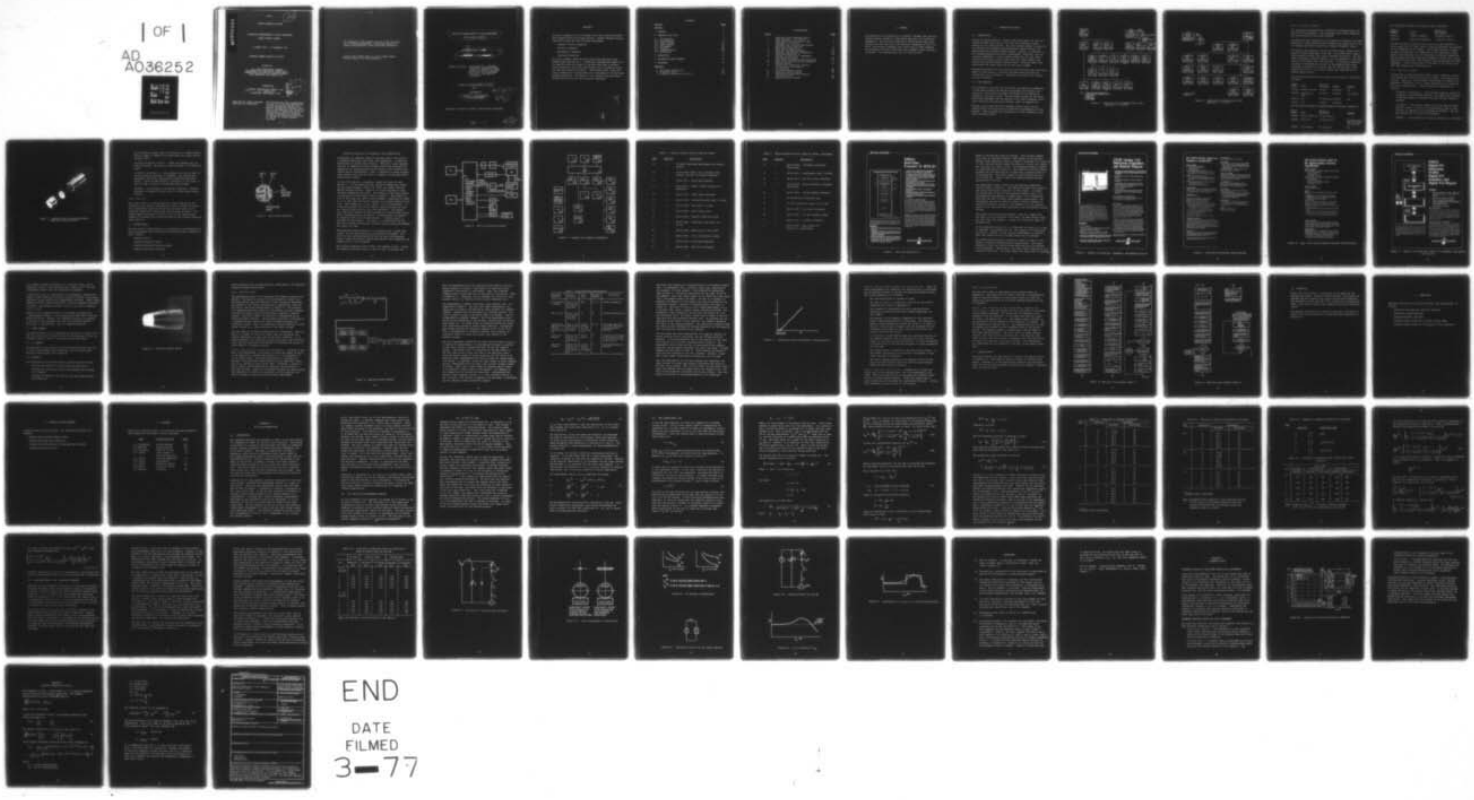

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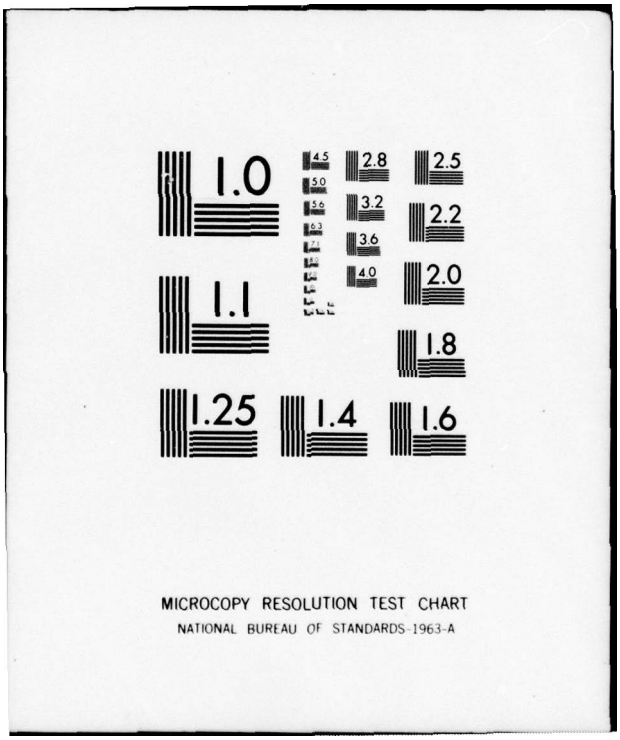
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SECOND QUARTERLY REPORT

PRODUCTION MEASUREMENT OF FUZE COMPONENTS UNDER DYNAMIC STRESS

11 AUGUST 1976 - 10 NOVEMBER 1976

CONTRACT NUMBER DAAB07-76-C-0032

PLACED BY

U.S. ARMY ELECTRONICS COMMAND
PROCUREMENT AND PRODUCTION DIRECTORATE
COMMUNICATION SYSTEMS PROCUREMENT BRANCH
FORT MONMOUTH, NEW JERSEY 07703

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CONTRACTOR

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PRODUCTION MEASUREMENT OF FUZE COMPONENTS UNDER DYNAMIC STRESS.

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SECOND QUARTERLY REPORT. no. 2,

11 AUG [redacted] — 10 NOV [redacted] 976,

OBJECT OF STUDY: DEVELOPMENT OF A COMPUTER CONTROLLED AUTOMATIC TESTER, CAPABLE OF TESTING AND TRIMMING THICK FILM ADJUSTMENT CIRCUITS AT THE RATE OF 3,000/HOUR

CONTRACT NUMBER (15) DAAB07-76-C-0032

(11) 9 Sep 76

PREPARED BY

(10) ARTHUR J. EISENBERGER
PHILIP KASZERMAN

(12) 71 p.

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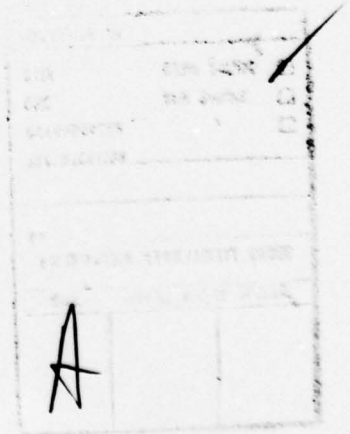
ABSTRACT

The major components for the dynamic test and correction system were ordered during the second quarter. Hewlett-Packard catalog items were chosen for the following subsystems:

- Computer control subsystem
- Stimulus subsystem
- Measurement subsystem
- Interface subsystem

The laser trimmer, which had been previously specified, was ordered from Quantrad Inc. In addition, mathematical models for the amplifier and oscillator of the M732 fuze were finalized (3,000 amplifiers and 3,000 oscillators will be tested to prove the test and correction system). These models plus a test and trim procedure were incorporated into a detailed set of real-time program flowcharts. The design of the revised fuze oscillator and amplifier circuitry was 90-percent completed.



CONTENTS

ILLUSTRATIONS

1. PURPOSE

The purpose of this program is to develop a dynamic test and correction system, capable of high-speed operation, for electronic assemblies. The circuits selected for verification under this contract are the oscillator and amplifier assemblies of the M732 Fuze. The contract requires that 3,000 units of each assembly be delivered, of which 2,900 have been trimmed to meet the specifications. The required test rate is 3,000 an hour.

2. NARRATIVE AND DATA

2.1 INTRODUCTION

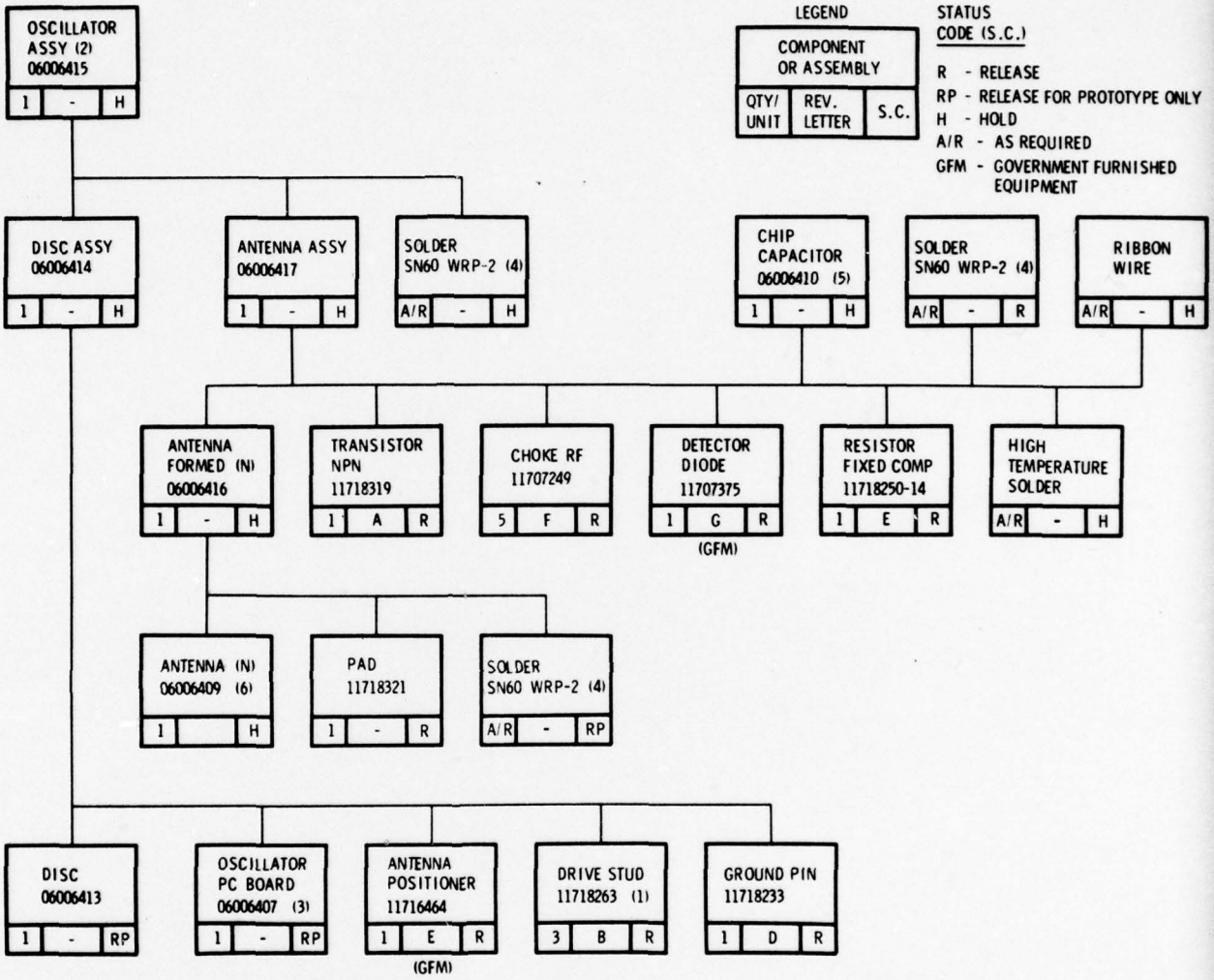
During the second quarter, catalog items were chosen for the test station system, which are in line with the conceptual system defined in the first quarter. The test station system is basically an extended low-frequency third-generation system based on the same principles as ECOM's EQUATE system. However, in addition to the computer-generated stimulus, measurement, interface, and calculation subsystems, a laser trimmer capability has been added. Virtually the entire system (other than the laser trimmer) was chosen from Hewlett-Packard catalog items. Purchase orders have been placed for these items and for the laser trimmer.

Mathematical models for the amplifier and oscillator were finalized. Based on these models, a detailed program design was made and incorporated into flowcharts. Redesign of the M732 fuze oscillator was continued.

2.2 FUZE REDESIGN

The redesign of the M732 fuze oscillator and amplifier assemblies, to make them suitable for dynamic measurement and testing, was continued. This effort included the electrical and mechanical redesign of the basic units. The new design allows for the necessary probe attachment and the design of the laser-trimmable oscillator capacitor and amplifier resistor (refer to Appendix B).

Figures 1 and 2 show the final assembly family trees for the modified M732 fuze oscillator and amplifier subassemblies in this program. These diagrams are expansions of those presented in the First Quarterly Report.



NOTES:
1. PARALLEL GROOVE CONFIGURATION REQUIRED.
2. SCHEMATIC AND PARTS LIST 06006408 ALSO RELEASED.
3. ARTWORK 06006412.
4. PER QQ-S-571.
5. ARTWORK 06006410.
6. ARTWORK 06006409.

Figure 1. ECOM Oscillator Assembly Family Tree (Revision 1, 11/15/76)

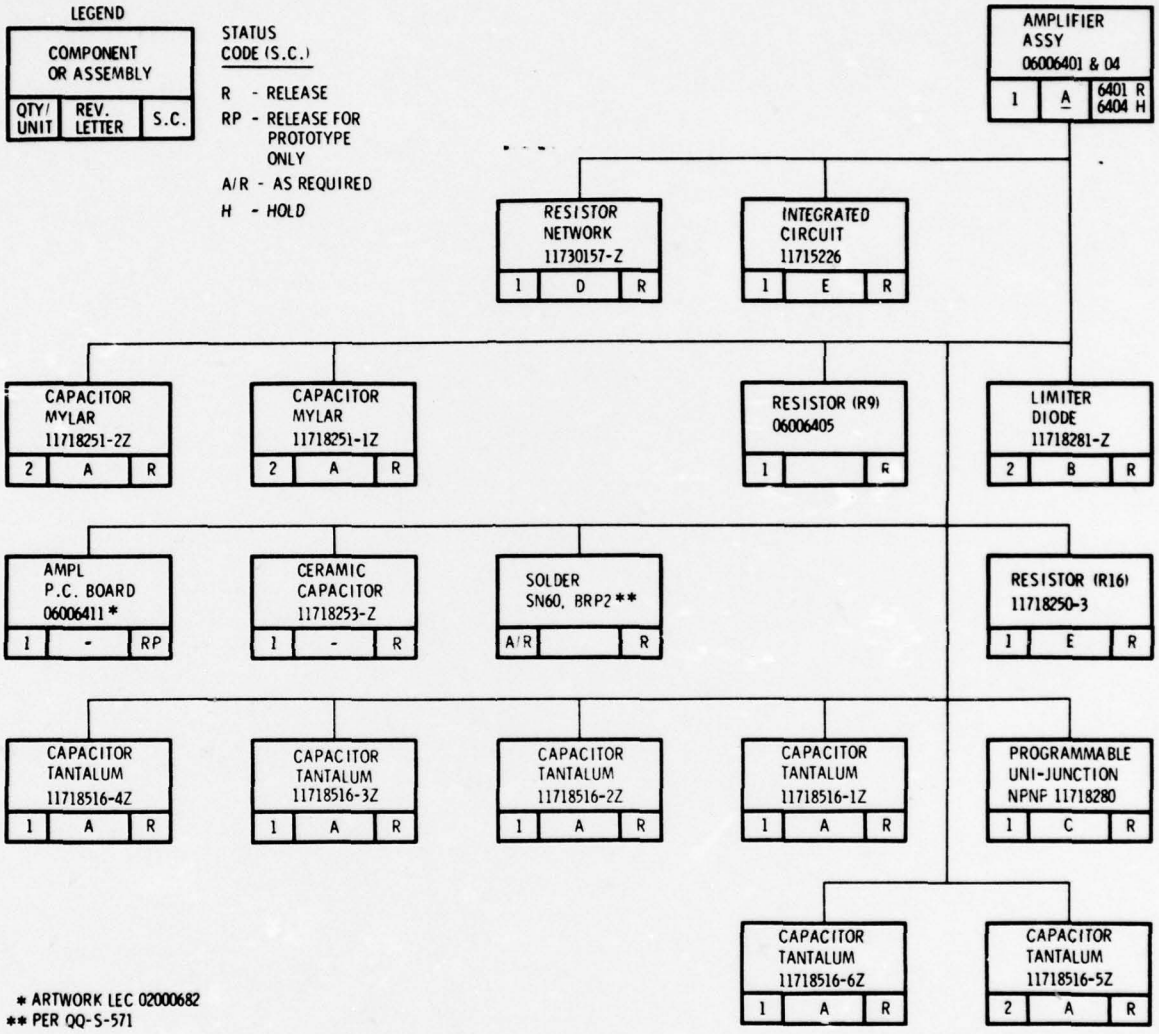


Figure 2. ECOM Amplifier Board Family Tree
(Revision 1, 11/15/76)

2.2.1 *Oscillator Assembly*

All electrical components were released for purchase before the end of the first quarter. The paragraphs that follow summarize the activity during the present quarter.

The HDL M732 fuze antenna-oscillator design (11716463-Z) has been modified to accept parallel plate ceramic chip capacitors for use in trimming oscillator sensitivity (doppler frequency output).

The initial chip-capacitor design was electrically tested and is presently being redesigned to provide a four-step binary capacitance variation rather than equal increment variations. The maximum differential capacity design is 2.3 picofarads for each capacitor on the ceramic chip (C21 and C22). A fractional picofarad variation is required as a result of the comparatively large variation in sensitivity with C21 and C22 and the need to set sensitivity to the $\pm$ 1/2-percent design goal required by the program specification.

The following drawings were released for prototype or production purchases:

Drawing Number	Title	Similar to HDL Drawing	Release	Comments
11716464	Antenna Positioner	11716464	Production	GFM
06006407	Oscillator PC Board	11718255-Z	Prototype	Plus artwork
06006413	Disc	Not applicable	Prototype	New
11718321	Pad	11718321	Production	-

The following drawings are approximately 90 percent completed:

Drawing Number	Title	Similar to HDL Drawing	Comments
06006416	Antenna Formed (N)	11718267-Z(Rev E)	-
06006409	Antenna (N)	11716463-Z(Rev E)	HDL drawing modified for ceramic chip capacitor
06006414	Disc Assembly	Not Applicable	New

The following drawings are presently being generated:

Drawing Number	Title	Similar to HDL Drawing
06006417	Antenna Assembly	11718268-Z (Rev F)
06006415	Oscillator Assembly	11718271-Z (Rev F)

The HDL oscillator printed circuit board has been modified to allow access for the laser beam to trim the capacitor chip mounted on the underside of the antenna. The antenna artwork is being revised, as necessary, to compensate for the additional capacitance of the chip and for the relocation of discrete components. The aluminum oscillator base disc (formerly a steel disc), which simulates the fuze body, was designed, and the drawings have been completed. The 70 units that will be used in the initial test have been manufactured (see Figure 3).

2.2.2 *Amplifier Assembly*

A comparison of amplifier-board family trees, presented in both this report and in the First Quarterly Report, show some modifications. These are minor changes incorporated to expedite the purchase of components, and to assure commonality of future HDL M732 fuze configurations. These changes are summarized as follows:

- 11718516-Z (Revision A). - The Tantalum capacitor drawing is identical to the 06006406 drawing. The number was switched to the HDL drawing to minimize confusion during component purchase.

- 11718253-Z. - The ceramic capacitor will be used in future HDL M732 fuzes. A value of 22 picofarads is used in this drawing, as opposed to 20 picofarads in 06006403. The new HDL drawing will be used in this program.

- 06006411. - This drawing is virtually identical to 11718276-Z.

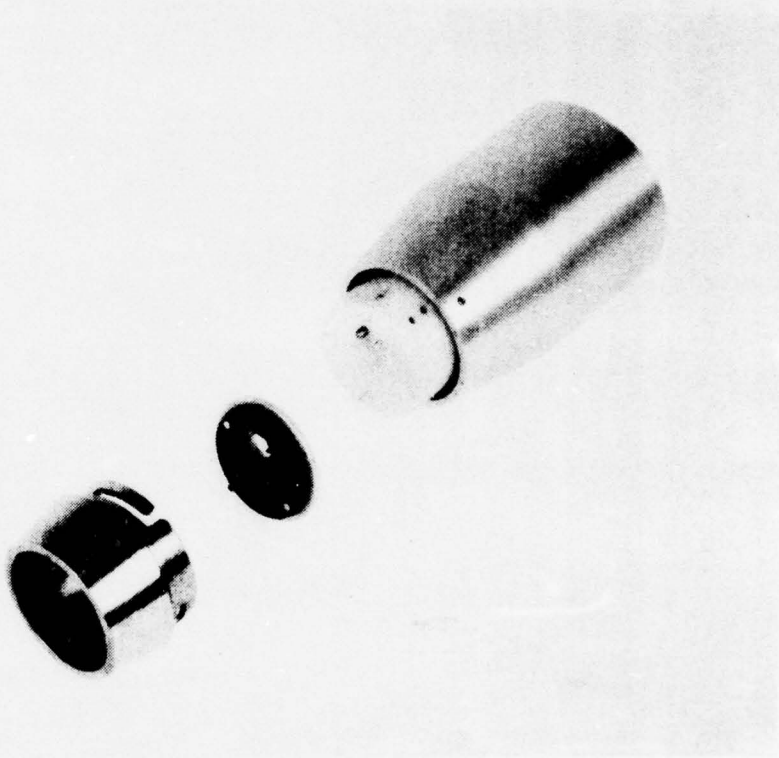


Figure 3. Exploded View of Positioner-Holder Detailing Steel Base Disc

The difference between these two drawings is a copper border, which is added to 06006411 for positioning the thick-film R9 resistor chip.

- 11715226 (Revisions C and E). - These two drawings are virtually the same. HDL plans on using Revision E in production fuzes.

- 11730157-Z (Revision D). - This drawing will also be used in HDL units and is identical to 06006402. The drawing was released by HDL after publishing the ECOM First Quarterly Report. Since the HDL drawing is available at this time, it will be used in place of the LEC-generated drawing.

- 06006404. - This drawing is 90 percent completed. 06006401 (Revision A) updates the parts list to include these modifications.

2.2.3 *Amplifier*

The latest version of the HDL amplifier board artwork has been modified on the reverse (noncomponent) side to provide an accurately reproducible mounting area for the resistor chip, with a resultant reduction in search time for the starting point. The etched copper rectangle will form a well for the liquid epoxy adhesive to restrict the liquid's flow during the mounting operation (see figure 4).

2.3 SYSTEM DESIGN

The test station system design is an extension of third-generation design principles, and it contains the following basic elements of such a system:

- Computer control
- Computer-generated stimuli
- Computer-controlled sampling system
- Computer-controlled interface

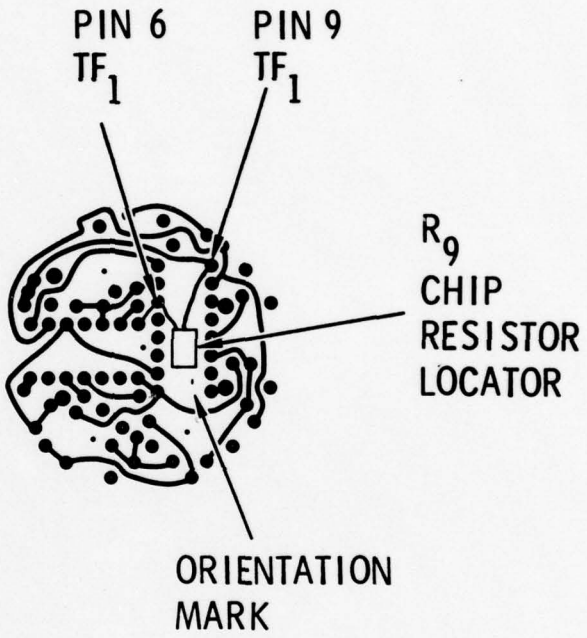


Figure 4. Back Side of Amplifier

. Computer calculation of parameters from sampled data

Furthermore, an important addition has been made in the form of a computer-controlled, real-time, trim capability. A laser has been chosen to perform this function. This unit, under computer control, is capable of either trimming thick-film resistors and capacitors or cutting printed wiring leads so that discrete components may be disconnected. Thus, in addition to being automatically tested, units can be tuned or trimmed to bring them within specification limits.

In the first quarter, a conceptual system was laid out (see Figure 5). In the second quarter, specific hardware was chosen. All the major hardware, except the laser, was chosen from the Hewlett-Packard catalog. Figure 6 is a block diagram in which the major components are shown. The letters in the lower corners of each unit, in this figure, refer to Table 1. This table is a list of the items with their catalog numbers. Referring to Figure 6, it is seen that the central computer is a Hewlett-Packard 2112A unit. This computer is a fast, modern, 16-bit minicomputer. It is being purchased with 32K of memory, which minimizes the need for program overlap during real-time operation. The computer will come with firmware for multiply/divide, floating-point arithmetic, double-precision arithmetic, 14 multiplexed I/O channels, an internal clock, and two DMA channels. A control panel is provided on the computer. This panel, in conjunction with the TTY, will provide the operator interface during program development and actual run time.

The operating system consists of a 4.9M byte disk, a paper tape loader, and the associated real-time executive programs. The disk will also provide storage for all the real-time programs. Figure 7 shows the Hewlett-Packard description that summarizes the capabilities of these programs.

The stimulus subsystem starts within the computer itself. Either by program or external entry, a table is made to describe the

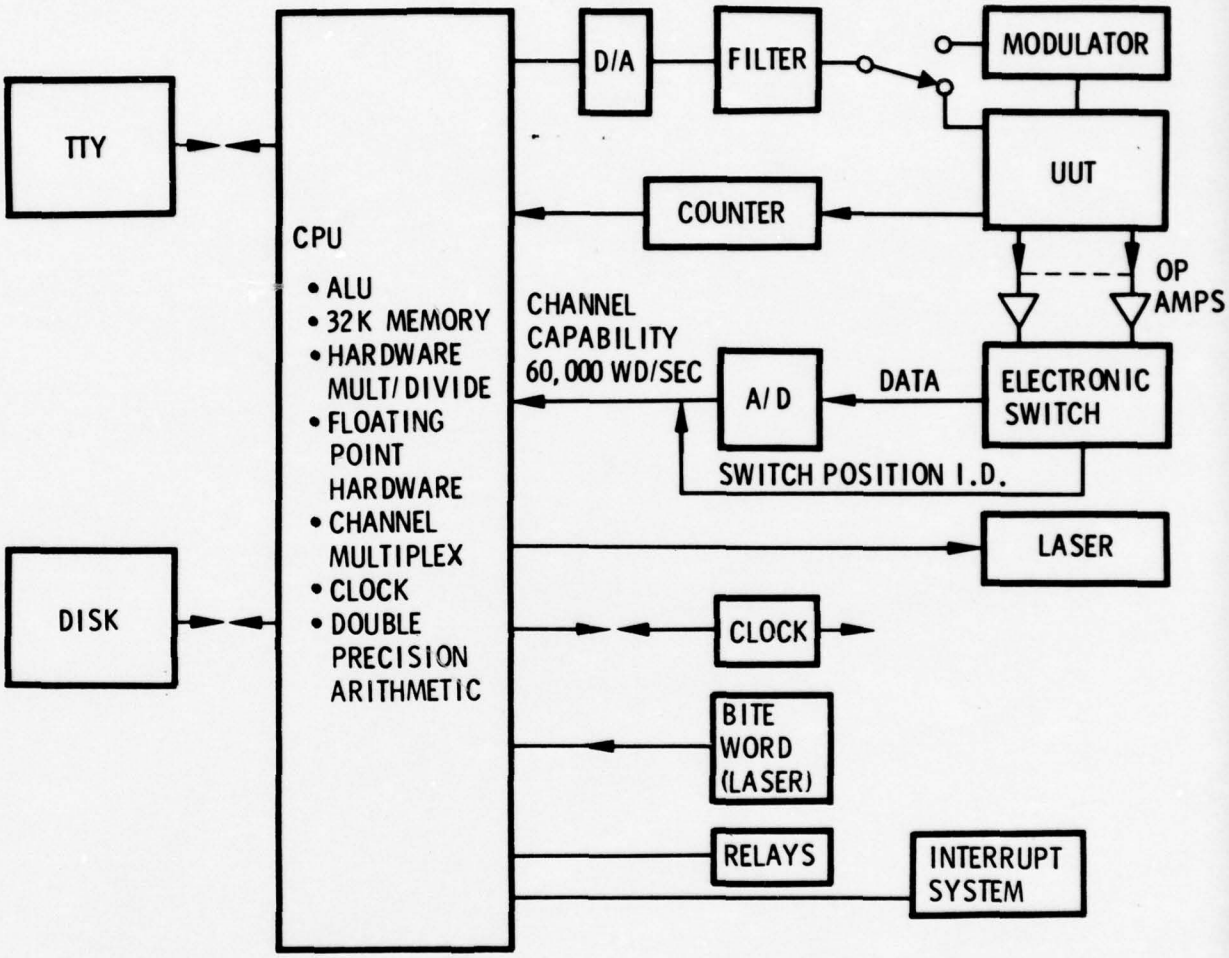


Figure 5. Test and Correction System

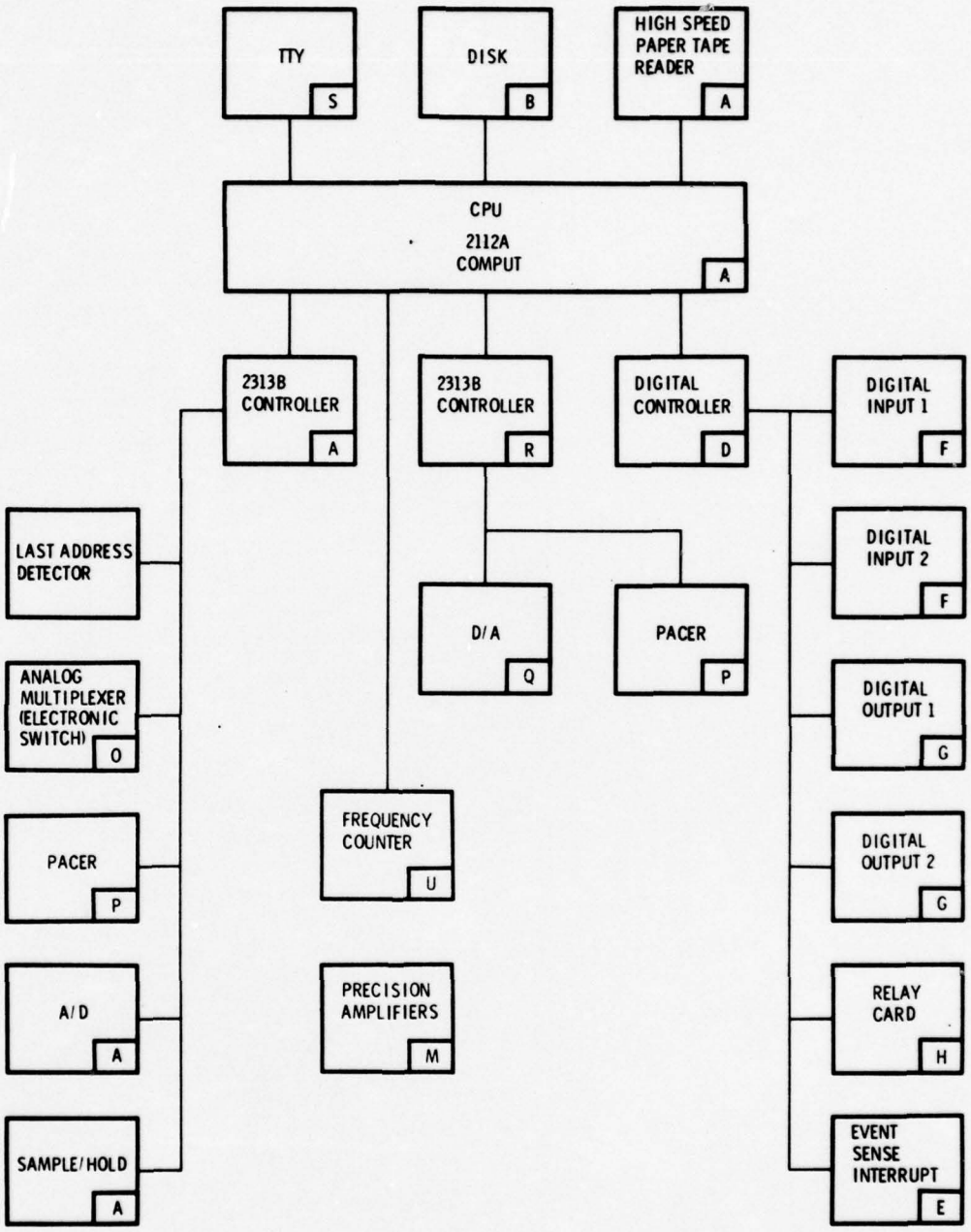


Figure 6. Computer and Computer Peripherals

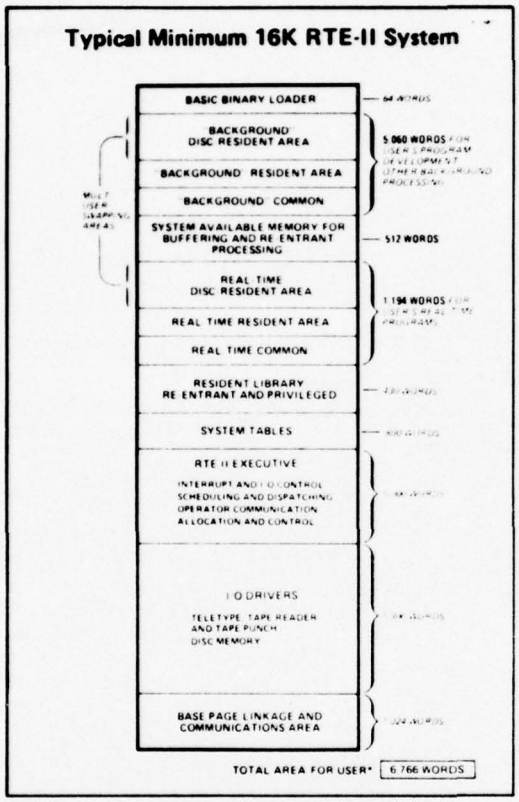
Table 1. Hewlett-Packard Catalog Items for Tester

Item	Quantity	Description
A.	1	HP 9603A High-speed Measurement and Control System.
B.	1	Option #A03: RTE-II with 4.9M Byte Disc, Cabinet, Fortran IV, System Libraries.
C.	1	Option #Y13: Batch Spool Monitor.
D.	1	Option #T17: 6940A (91063A) Digital I/O Subsystem.
E.	1	Option #J17: Event Sense Interrupt.
F.	2	Option #J16: Isolated Digital Input, 12 bits.
G.	2	Option #K04: TTL Output, 12 bits.
H.	1	Option #K05: Relay Output Card.
I.	1	Option #P24: Replace 2108A with 2112A.
J.	1	Option #R00: Teleprinter and Local I/O, 10 cps.
K.	1	Option #005: Additional I/O for 2313B.
L.	1	Option #021: 10 ft. Differential Cable.
M.	3	Option #025: 2471A Data Amplifier.
N.	1	Option #026: Case for 2471A Cards

Table 1. Hewlett-Packard Catalog Items for Tester (continued)

Item	Quantity	Description
O.	1	Option #008: 16-Channel High Level Multiplexer.
P.	2	Option #011: Programmable Pacer (12755A).
Q.	1	Option #013: D/A Dual 12-bit Converter.
R.	1	Option #558: Second 2312B-001 Integrated into 9603A.
S.	1	Option #P12: 16K Word Memory Expansion.
T.	1	HP 59310B HP-IB Interface Card.
U.	1	HP 5341A Frequency Counter to 4.5 GHZ.
V.	1	Option #002: Rear Panel Connectors
W.	1	Option #003: 1.5 GHZ Frequency Range.
X	1	Option #011: I/O ASCII Interface
Y	1	Option #908: Rack Flange Kit; HP Part No. 05326-60046.

92001A Real-Time Executive II (RTE-II)



Hewlett-Packard's Real-Time Executive II (RTE-II) is a time- and event-scheduled, disc-based, foreground-background real-time multiprogramming system for use in 9600 series systems.

Features

- **Foreground and background multi-user swapping partitions.**
- **Operation in as little as 16k of CPU memory, or up to 32k for user's real-time applications and RTE-II supported capabilities.**
- **Supports cartridge disc subsystems providing 4.9 to 118 Mbytes of on-line storage with optional file management to provide ample capacity for programs and a fast-access data base.**
- **Supports IMAGE/1000 Data Base Management System for more efficient use of data files.**
- **Concurrent processing and program development in FORTRAN II/IV, Conversational Multi-User Real-Time BASIC (optional), ALGOL, and HP Assembly language.**
- **Multi-terminal access to all system resources, serving multiple users concurrently.**
- **Optional input/output spooling to disc to speed throughput without excessive use of CPU memory for buffering.**
- **Optional interactive editor to aid program development.**
- **Supports coordination of distributed multiprocessor communication networks.**
- **Supports data communication with IBM 360/370 or HP 3000.**

REAL-TIME MULTIPROGRAMMING

The RTE-II system supervises the execution of multiple programs including user's programs for measurement, control, data processing, and data reporting, and RTE-II based programs (editor, compilers, assembler, etc.) for concurrent program development. Multiprogramming gives the user the ability to match the frequency and timing of programmed task actions to the diverse needs of real-time applications in research and manufacturing.

Scheduling. The multiple programs in the RTE-II system are executed on scheduled basis, as shown in Figure 1. RTE-II lists all programs in order of priority that are ready for execution. Programs are placed in this list when it is time for them to run, in response to external event interrupt, and when execution is requested by another program or by the operator. RTE-II recognizes priority levels from 1 through 32767 and program execution may be scheduled on time resolutions as small as tens of milliseconds.

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Figure 7. Real-Time Executive II

shape of the desired stimulus waveform. Upon program command, this table is outputted through a DMA channel to the Hewlett-Packard 2313B controller shown in Figure 8 (labelled R in Figure 6). In turn, the multiplexer routes the words to a 12-bit D/A converter, and then to a small filter. The stimulus system is capable of outputting digital words at a rate limited by the DMA channel, although the D/A specification is given for a settling time of 20 microseconds. The actual output is controlled by the *pacer* (P in Figure 6). Figure 9 shows the Hewlett-Packard catalog description of the D/A.

The measurement system starts with the precision amplifiers (unit M) shown in Figure 6. The amplifier outputs are routed to the analog multiplexer labelled O in this Figure. In effect, the multiplexer is part of the switching system, since it is programmed by the computer to sample from 1 to 16 consecutive positions and then to repeat these samples continuously. The multiplexer can also be used in a mode in which a sequence of arbitrary positions, stored in the computer, will be executed. Figure 10 is a more detailed description from the Hewlett-Packard catalog.

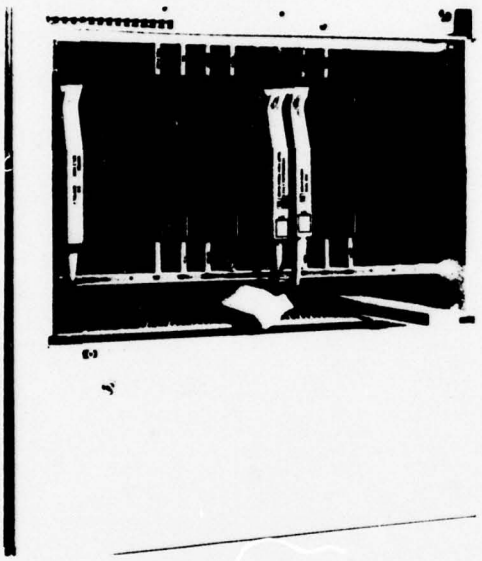
The output of the analog multiplexer is fed to a sample-hold and then to an A/D converter; from there, the DMA channel reads the words into the computer. A pacer (O) accurately times the transfer rate.

If the specified accuracy of $\pm$ 0.09-percent full-scale $\pm$ 1/2 LSB is required, the maximum rate into the computer is 45,000 words per second. However, if the accuracy requirement is removed, a peak rate limited by only the DMA channel may be achieved.

The Hewlett-Packard digital controller shown in Figure 11 (D in Figure 6) handles low-speed digital input/output. The output commands to the laser and the laser BITE word will run through this multiplexer. Additionally, the event sense interrupt is controlled by this unit. The event sense unit can be set to interrupt

HP DATA SYSTEMS

2313B Analog I/O Subsystem, Expanders, and Related Plug-ins



The 2313B Analog I/O Subsystem consists of control, sampling, and analog-to-digital conversion modules in a mainframe providing at least two spaces for analog I/O plug-ins. It also includes a separate power supply, a computer interface card with interconnecting cable, and software appropriate to the operating system in which the subsystem is used. It is designed for rack-mounted operation only. The 2313B is standard in 9603A, 9604A, 9610, and 9611A Measurement and control systems and is offered for the addition of analog I/O capability to other systems configured around HP 96MX System Controllers on HP 2100A or later HP 2100 series Computers.

Features

- 12-bit resolution.
- Analog I/O plug-ins available with screw-terminal industrial connection assemblies.
- High-level (±10.24V fs), solid state S.E. or diff. analog input at scanning speed up to 45 kHz.
- **Low-level (± 10 to 800mV fs), solid state analog input at scan rates to 8 kHz*, signal plus CMV ≤ 10V.**
- **Low-level (± 10 to 200 mV fs), relay analog input at scan rates to 150 Hz*, 200V CMV.**
- **Solid-state or relay switched 2.5, 5, 10, 20, 25, and 50 mA analog current input multiplexing (industrial version only).**
- High-accuracy 12-bit (±10.24V, 20mA) analog outputs.
- Plug-in pacer available for precision timing of analog I/O.
- Input/output capacity expandable to 528 differential analog inputs or 44 analog outputs, or combination of inputs and outputs.
- Field expandable.
- Software drivers and interface routines for BCS, RTE-B, RTE-C, RTE-II, and RTE-III operating systems.

EXPANDABILITY AND CAPABILITIES

The expandability and capabilities of the HP 2313B subsystem are summarized in diagram, overleaf.

Easily Installed

With the user's choice of appropriate analog I/O cards, the subsystem is a complete package, virtually ready to use as soon as it is delivered. Simply rack mount the subsystem, plug one interface card into the computer, and connect the cable. The subsystem needs only to be integrated into the software operating system (BCS, RTE-B, RTE-C, or RTE-II) of the computer to be ready for programmed operation. When it is ordered as part of a complete system, Hewlett-Packard does the integration for you.

In addition to the driver software used in normal operation, the subsystem includes a unique verification program. This is an interactive program in which the operator commands any mode of operation via the system's keyboard input unit or paper tape reader. An easy-to-follow printout or display of the results is provided. Because it is extensive and easy to use, this program can substitute for application programming during the early stages of system setup. It will thus save time and effort, at the same time confirming correct operation of the subsystem.

*These are hardware rates subject to response degradation that depends on other activity in the system.

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Figure 8. Analog I/O Controller, Expanders, and Related Plug-ins

HP 12751A/91110A High-Level Multiplexer Specifications

Hardware Supplied
HP 12751A High-Level Multiplexer:
1. High-Level multiplexer card.
2. Mating connector.

HP 02313-60007 Single-Ended Input Cable:
16-foot cable, terminated with high-level multiplexer mating connector at one end, unterminated at source end.

HP 02313-60008 Differential Input Cable:
16-foot cable, terminated with high-level multiplexer mating connector at one end, unterminated at source end.

HP 91110A High-Level Multiplexer, Industrial Version:
1. High-level multiplexer card.
2. Screw-terminal connection assembly.

Number of Inputs
16 differential or 32 single-ended (single-ended operation applies only to 12751A, not to 91110A which is limited by its connection assembly to 16 differential inputs).

Full Scale Input
+10.235V to -10.240V

Overall Accuracy of Multiplexer, S&H, and ADC
With Respect To: source used for calibration.
Conditions: source resistance < 100 ohms.
Factors Included: 3 sigma noise; linearity, offsets, 8-hour stability; gain, calibration transfer, and dynamic response errors; and effects of ±10% line voltage variation and ±5°C variation from calibration temperature.
Accuracy: ±0.09% fs ±1/2 LSB (subsystem without expanders); 12764A expander adds ±0.05 fs and 12765A expander adds ±0.06% fs.
Temp. Coeff: ±0.0026% fs/°C.
Long-Term Drift: ±0.06% fs, maximum, in 30 days.

Throughput Rate to Buffer
To 45 kHz* via Dual-Channel Port Controller (DCPC), assuming no interrupts from higher priority devices, no other machine cycles used for DCPC, no more than one level of indirect addressing, and no chaining of indirects in non-DCPC operations. Includes high-level multiplexer switching, S&H sampling, and ADC conversion times. To 10 kHz in BCS-based system not using DCPC.

Aperture Time
50 nanosec, peak-to-peak time variation, reading-to-reading if subsystem is paced by HP 12755A Programmable Pacer. Includes S&H aperture and pace pulse jitter.

*This is a hardware rate subject to response degradation that depends on other activity in the system.

Source Resistance
1kΩ, maximum, balanced or unbalanced.

Input Impedance
Selected Channel: > 5MΩ shunted by < 60pF (1 HLMPX card); > 3.3MΩ shunted by < 70pF (9 HLMPX cards); > 2MΩ shunted by < 120pF (33 HLMPX cards in fully-expanded subsystem.
Non-Selected Channel: > 50MΩ shunted by < 10pF.
Power Off: > 500kΩ, all channels.

Pumpout Current Offset
Offset due to HLMPX switching transients stored on input cable capacitance < 1000pF: < 0.05% fs at 45 kHz, with 500Ω source resistance, ±10.3V inputs (differential + common mode), 528 inputs in subsystem.

Crosstalk Rejection
Between Inputs to Same HLMPX Card: 80 dB.
Between Inputs to Different HLMPX Cards: 120 dB.
Conditions: dc to 1 kHz, 1kΩ source resistance.

Common Mode
Rejection: 80 dB, dc to 60 Hz, 1kΩ source resistance, using differential input.
Return: ≤ (10 kΩ + 10 μH) with up to 125 feet of HP part No. 8120-1781 input cable for differential inputs. To 10Ω, maximum + 10 μH, maximum, low to power common, for single-ended inputs.

Maximum Input
For Rated Accuracy: ±10.5V diff. + common mode, or ±10.24V high-to-common, single ended input.
Without Damage: up to ±15V, any input line to chassis.

Weight
HP 12751A: 2 lb (0.91 kg).
HP 91110A: 4.5 lb (2.05 kg).

Figure 9. High-Level Multiplexer Specifications

HP 12757A/91113A Dual 12-Bit Digital-Analog Converter Specifications

Hardware Supplied

HP 12757A Dual 12-Bit Digital-to-Analog Converter (DAC):

1. Dual 12-bit DAC card.
2. Mating connector.
3. Dual-DAC test routine.

HP 91113A Dual 12-Bit Digital-to-Analog Converter (DAC), Industrial Version:

1. Dual 12-bit DAC card.
2. Screw-terminal connection assembly.
3. Dual-DAC test routine.

Number of Outputs

Two outputs per DAC card.

Output

Signal: +10.235V to -10.240V, 0 to 20mA, short circuit proof.

Load Regulation: ±0.05% fs, maximum, 0 to 20mA.

Load Capability: resistance > 500Ω, capacitive load to 0.002μF will not cause instability.

Resolution: 5mV.

Accuracy at 25°C (77°F): ±0.025% fs, 0 to 5mA output.

Temp. Coeff: ±400μV/°C (±222μV/°F), maximum.

Stability: 1.5mV, maximum total drift for 24 hours, after 1 hour warmup.

Settling Time: 50μsec, maximum to within ±0.05% of final value.

Ripple and Noise: 2mV p-p, maximum in 0 to 100kHz bandwidth. Transients with 10mV peak amplitude, and 2μsec duration may occur when either channel is programmed.

Remote Grounding

"Low" output lead may be grounded remotely, provided ground voltage does not differ from system ground by more than ±2V. (DAC output voltage plus common mode voltage must be between +10.235V and -10.240V).

Display Interface

Blanking Pulses: +10V to -10V, high, and +1V to -1V low.

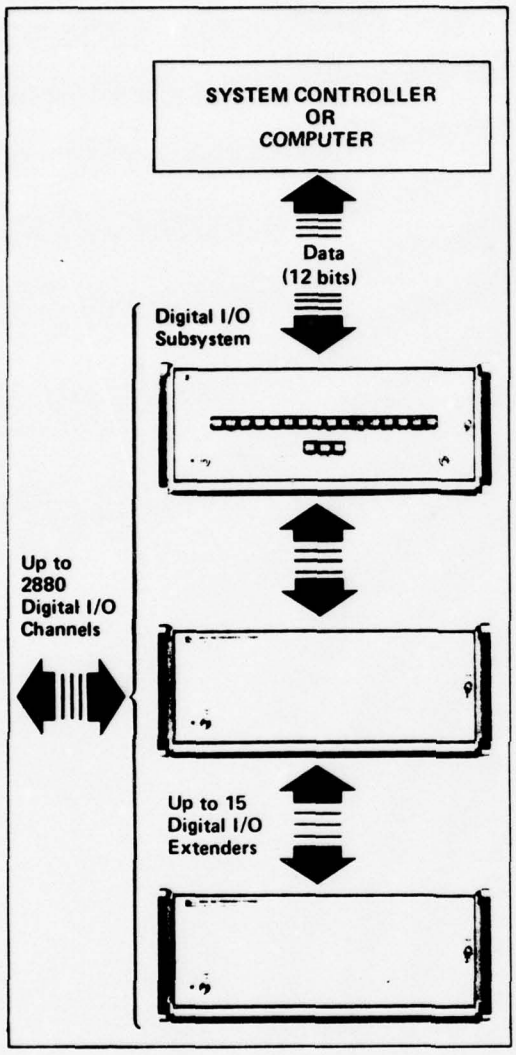
Blanking Pulse Duration: 250nsec/4μsec, jumper selectable.

Display Erase: NPN transistor closure to ground for 1 second; 25V max. open circuit, 16mA, max. sink.

External Flags: TTL compatible and +10V inputs.

Figure 10. Dual 12-Bit Digital-Analog Converter Specifications

HP DATA SYSTEMS



The 91063A Digital I/O Subsystem consists of a 6940B Multiprogrammer and interface for HP 2100A and later HP 2100 Series Computers. It is standard in 9610 and 9611A Industrial Measurement and Control Systems and is offered for the addition of digital I/O capability to 9602A, 9603A, and 9604A Scientific Measurement and Control Systems.

91063A Digital I/O Subsystem, 91140A Digital I/O Extender, and Digital I/O Plug-ins

Features

- **Capacity expandable from 15 to 240 12-bit I/O card slots (up to 2880 digital I/O channels)**
- **Uses only one computer I/O channel**
- **Wide choice of digital I/O capabilities**
- **Software supplied for HP 2100 and 9600MX series computer systems**
- ***Easily installed and serviced***

EXPANDABILITY

The basic capacity of the subsystem is 15 card slots for 12-bit I/O cards. Through the addition of 91140A digital I/O extenders, this capacity can be increased to 240 I/O card slots (15 in the subsystem mainframe and 15 more in each of 15 I/O extenders). The entire digital I/O subsystem connects to the computer via a single 16-bit microcircuit duplex register interface.

WIDE CHOICE OF CAPABILITIES

Subsystem capabilities are offered as modular plug-in cards, including 12 channel status inputs, 12-channel event sense inputs, and event counter input. Both solid-state and relay contact outputs providing 12-channel capacity are offered. Other digital output choices include a stepping motor controller, a programmable timer, a stall alarm, and a frequency reference. The subsystem can also be equipped with both digital-to-analog current and voltage converters, each providing 12-bit resolution.

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Figure 11. Digital I/O Controller, Digital I/O Extender, and Digital I/O Plug-ins

the computer, based on matching a bit reference word. Since there are 12 bits in the reference word, there are 2^{12} (or 4096 independent events) that can interrupt the computer.

A relay card (unit H) consisting of 12 single-pole, single-throw relays is also computer-controlled through the digital multiplexer. Additional relay cards can be inexpensively obtained. These relays, together with the analog multiplexer, form the computer-controlled interface. The frequency counter (unit U) can read rf frequency up to 1.5 GHz.

Except for the frequency counter, this system is essentially a low-frequency system. It is limited by the DMA rate to 600,000 words per second. However, the frequency range can be extended to include rf and microwave test and trim by adding external buffering, rf synthesizers, and an rf spectrum analyzer.

2.4 LASER TRIMMER

The Quantrad Model 1021 is scheduled for delivery in January 1977. Two field trips were arranged to monitor the progress in both the mechanical/optical and the electronic realization areas.

2.5 RF CHAMBER

The drawings for the prototype positioner-holder device (for use in the rf load chamber) were completed, and the detail parts have been manufactured (see Figure 12).

2.6 ANALYSIS

The objectives of the second quarter analysis were as follows:

- Finalize the models of the amplifier and oscillator.
- Finalize the test-signal design and determine the voltages to be sampled.
- Finalize the method to be used for the real-time analysis and prediction.

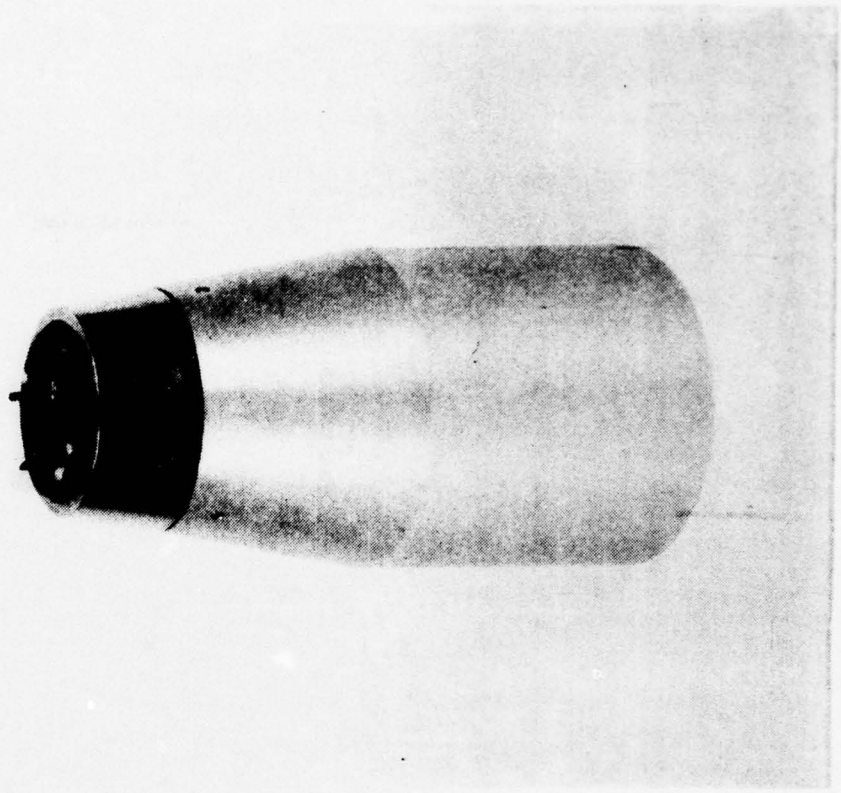


Figure 12. Positioner-Holder Device

These objectives were accomplished and, additionally, the required program flowcharts were drawn.

2.6.1 *Amplifier Model*

The mathematical model of the amplifier was firmed up during this quarter. The model is similar to previous models, except that the differential amplifier/detector is more completely described. An analysis of the circuit diagram and an experimental verification led to the block diagram shown in Figure 13. The differential amplifier/detector consists of two halves; one half responds to positive signals, while the other half responds to negative signals. The first element in each half is represented by an ideal half-wave rectifier. The half-wave rectifier is followed by a threshold device, which only allows voltages exceeding the threshold to pass. This is followed by a current generator, whose output current is a linear function of the input voltage.

The two sides of the detector/amplifier are independent. Measurements on a number of units have shown that the thresholds and current generators for each side can be quite different. It is these thresholds, the difference between the sides, and the M-wave input that has complicated the problem of adjusting the height of burst within a 1.2-second interval.

2.6.1.1 *Amplifier Test Signals and Measurements.* - Because of the short time requirement (1.2 seconds) in which the height of burst of the amplifier is tested and adjusted, it is not possible to use an M-wave input. The M-wave lasts about 1.4 seconds and, because of the nonlinear characteristics of the amplifier, would have to be applied at least three times. Therefore, a series of short signals, which determine the amplifier characteristics, have been devised. Based on the measured response to these signals, the response to an M-wave is calculated, and the amplifier can then be trimmed to meet the height-of-burst requirement.

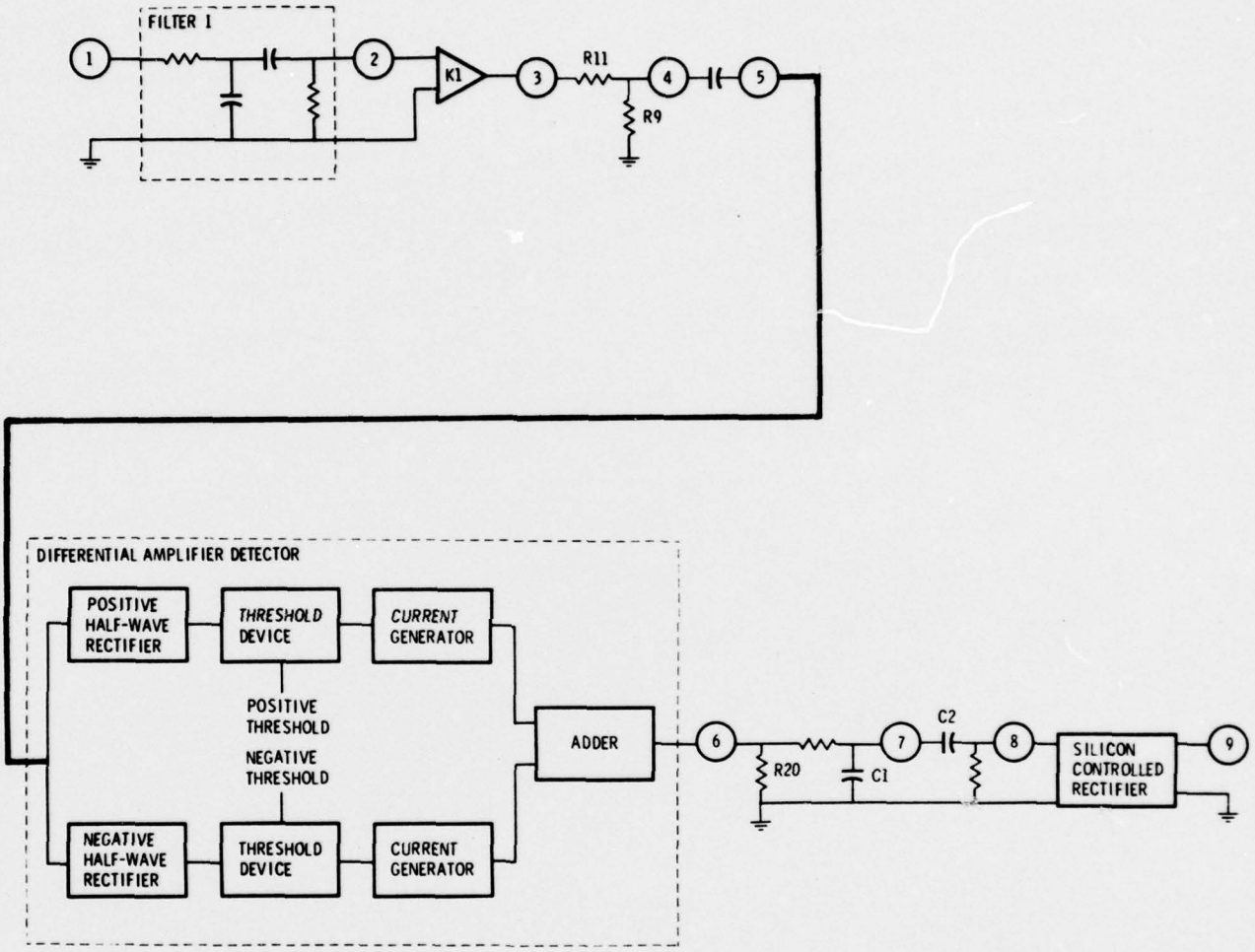


Figure 13. Amplifier Block Diagram

Both the measurements and the calculation are based on the frequency response of filter 1 (see Figure 13) being very broad compared to the carrier of the M-wave. Thus, the transient response time is much less than a half-cycle of the carrier (refer to Appendix C). Therefore, we can consider the filter as a gain element, which is a function of the carrier frequency only.

The measurements, hardware conditions, input signals, etc., are summarized in Table 2. For the first three measurements, the capacitors in filter 2 are shorted by relay contacts via computer command. Resistor R20 is paralleled by a 100-ohm resistor, the value of which is known to be better than 0.01 percent. This is accomplished by computer command. The first measurement determines the dc attenuation of the divider, consisting of R9 and R11 (see Figure 13). No input signal is required because the normal bias conditions provide dc across these resistors. The measurement simply consists of taking one reading of V3 and one of V4. This is accomplished via computer commands, which connect the electronic switch to these test points, and reading in the sampled voltages.

The next measurement determines the gain from the input to point 5. To obtain this measurement, a known Doppler CW signal is applied to the input, which is handled entirely through the computer system. A sine-wave table is outputted via the DMA channel to the D/A, then to the filter, and then to the amplifier input. Since the signal chosen is large enough for the S/N ratio to be extremely high, measurements need only be taken for approximately five cycles. In addition, since the input signal is under computer control, measurements will be taken over an exact integral number of cycles. Thus, only a small number of samples need be taken. It is planned to take a total of 100 samples. The adequacy of this number will be verified by simulation. Measurements are entirely under computer control, i.e., the electronic switch is set to point 5, the voltage is sampled, A/D conversion is performed, and the computer accepts successive samples.

Table 2. Measured Amplifier Characteristics

Measurement Objectives	Hardware Conditions	Input Signal	Measured Voltages	Calculations
Dc attenuation of divider	Short C1,C2; parallel R20 by a small resistance	None	V3, V4	Divider attenuation
Gain to point 5	Short C1,C2; parallel R20 by a small resistance	CW	V5	Rectified average of ac
Positive and negative threshold and current generator	Short C1,C2; parallel R20 by a small resistance	Delayed positive and negative ramps at V6	V5, V6	Least mean square fit to line to give thresholds and current generators
Filter step response	Remove short from C1, C2, and small R from across	Step of carrier	V8	Preliminary calculation of step input to filter A, p1, p2 of u(t), and C and D of h(t)
SCR firing voltage	Remove short from C1, C2, and small R from across R20	Increase carrier step sign to maximum	V8	*Spike* determination at SCR gate

The third test measures the characteristics of the detector/amplifier. To accomplish this, a positive input ramp, generated by the computer, is first applied. This produces an approximate ramp at point 5. During the application of the ramp, V5 and V6 are sampled. Since the signal chosen is far above the noise level, only a few samples need to be taken. The use of 20 samples is planned; the adequacy of this amount will also be checked by the simulation program. Typical I/O characteristics are shown in Figure 14. This data is used to find a least-mean-square fit to a straight line, using a typical linear regression program. The threshold is the intersection of the line (see Figure 14) with the horizontal axis. The slope of this line is equal to the voltage gain with the precision resistor load. By dividing the voltage gain by the value of this resistor, the computer generates the value of the current generator. By outputting a negative ramp, the values of the threshold and current generator for the negative half are similarly obtained by the computer.

For the fourth and fifth measurements, the computer removes the shorts from the filter capacitors, and the 100-ohm precision resistor. A carrier modulated step is then applied at the input. This results in a full-wave rectified step at point 6. The magnitude of the V6 step can now be calculated by the computer, since all the parameters preceding this point are known. Voltage samples are then taken at point 8. Three samples are needed to solve for the constants in the step response. However, a somewhat larger number (determined by simulation) will be used.

Once the measurements for the step response are completed, the input voltage is raised high enough to guarantee the firing of the SCR. V8 is sampled. When the SCR fires, the fire pulse interrupts the computer and the program halts the reading of V5. The data is then examined to determine the firing voltage. This completes the process of taking measurements on the amplifier.

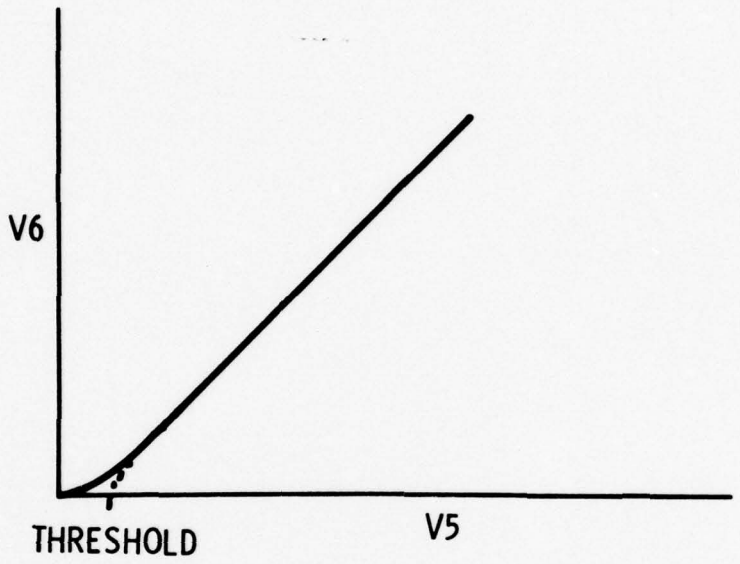


Figure 14. Differential Amplifier/Detector Characteristics

2.6.1.2 *Height-of-Burst Analysis and Gain Prediction.* - When the above measurements are completed, the required gain is calculated by the computer program to achieve the specified height-of-burst. The overall approach is as follows:

- The specified M-Wave is assumed as input.
- The gain to point 5 is taken as a function of the carrier frequency only (refer to Appendix C).
- The threshold is subtracted from the rectified M-Wave (positive and negative halves are treated separately and then added).
- The average (or dc frequency component) of the rectified M-Wave, minus thresholding, is calculated. The average is used as current-generator sources for filter 2, as shown in Figure 13 (the carrier frequency and its harmonics will be filtered by the first RC; thus, they will not affect the time at which the SCR fires).
- A convolution is performed between the rectified average and the impulse response time to determine the filter voltage output at the time the fuze should fire. To ease programming, a look-up table of convolution integrals vs filter parameters will be used.
- The filter output is compared to the SCR firing voltage. If the output and voltage are not within 0.05 percent of each other, the gain is rescaled.
- The above program subroutines are repeated, using the new gain, until the filter output and the SCR firing voltage differ by less than 0.05 percent.

2.6.1.3 *Amplifier Test and Trim.* - Trimming R9, to bring the actual gain to the required gain, will be accomplished in two steps. The first step will be to calculate the required length of cut to within several percent. During the second step, a small shadow cut will be taken while monitoring the gain. Cutting will stop when the gain is set to 0.05 percent.

2.6.2 *Oscillator Model*

The oscillator model is described in much greater detail in Appendix A. This model will be used to develop a two-dimensional table of required changes in capacitance, which will meet the sensitivity specification vs the actual measured sensitivity and Rf frequency.

2.6.2.1 *Oscillator Test Signal, Measurements, Analysis, and Test and Trim.* - The test signal will be a CW signal at the center of the Doppler passband. The signal will be outputted by the computer to the Rf modulator. At the same time that the signal is output, the sensitivity (i.e., the doppler output voltage) of the oscillator will be sampled 10,000 times for 0.1 seconds. The Rf frequency will then be read in. The sampled data will be used to compute the Discrete Fourier Transform (DFT) at the CW frequency. The required change in capacity will then be found in the table mentioned above. The laser, which is under computer control, will then trim the capacitor pad. The sampling, DFT, table look up, and trim process is repeated until the sensitivity is within 0.25 percent of the specification. This measurement and computation will be repeated at the ends of the Doppler passband.

2.7 PROGRAM DESIGN

The program design has been updated to reflect the analysis given in Section 2.6. The flowchart shown in Figure 15 reflects this update. Although it is not specifically shown in the flowcharts, there will be an overlap between outputting test signals, inputting data, and calculations.

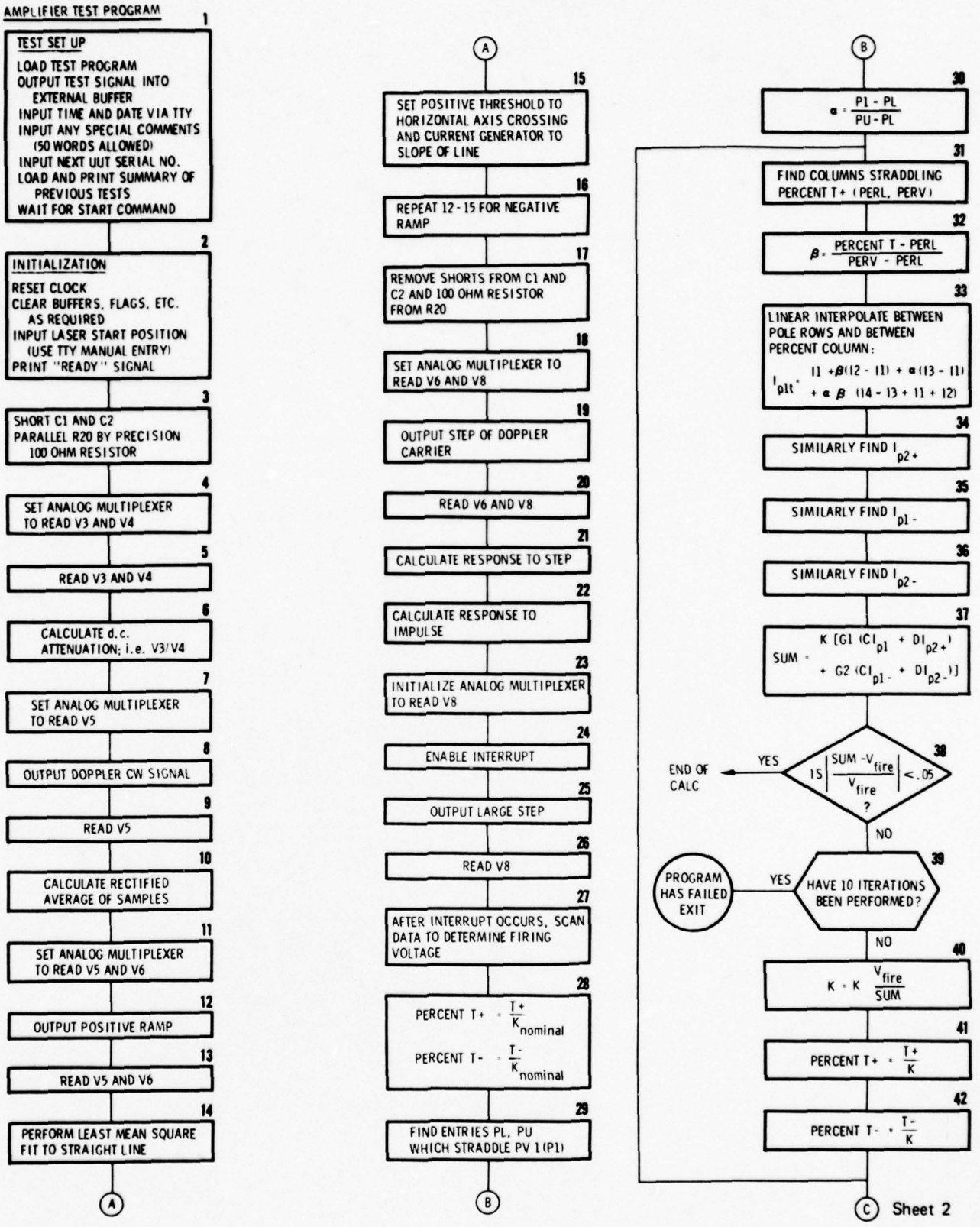


Figure 15. Amplifier Test Program (Sheet 1)

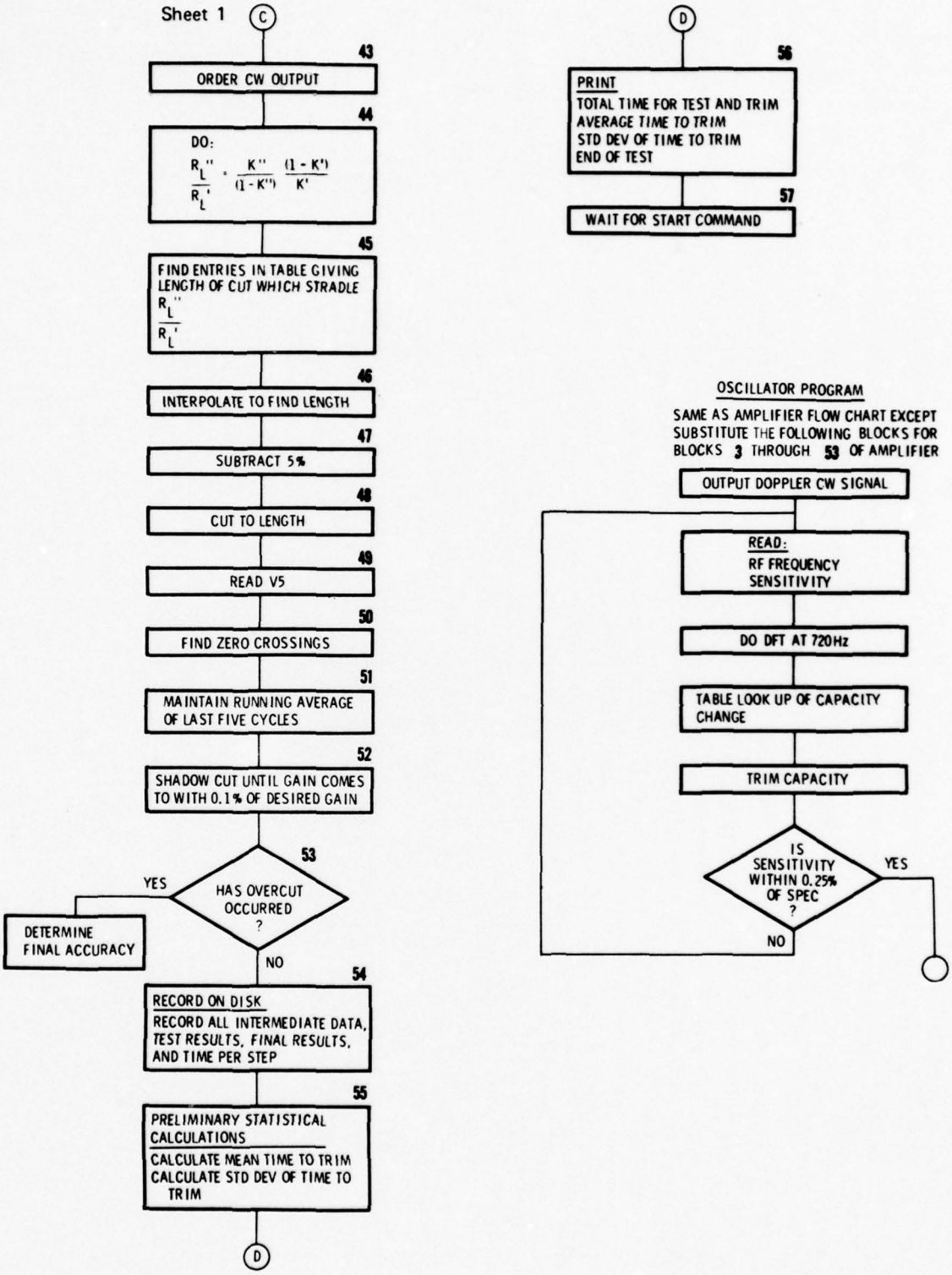


Figure 15. Amplifier Test Program (Sheet 2)

2.8 SIMULATION

During the first quarter, a simulation of the amplifier was designed and coded. During the second quarter, the program was debugged and the amplifier was shown to be properly simulated. The simulation of the oscillator will consist of an experimental model, using look-up tables that summarize oscillator characteristics.

The complete simulation will link the oscillator and amplifier models with the real-time test program simulation described in Section 2.7.

3. CONCLUSION

The major objectives of the second quarter were accomplished, as follows:

- Oscillator and amplifier analysis completed.
- Simulation program designed.
- Subsystem designs completed.
- Purchase orders placed for all major system items.
- Purchase orders placed for 95 percent of fuze components.

4. PROGRAM FOR NEXT QUARTER

During the next reporting period, the following activities are planned:

- Receive major system hardware items.
- Receive prototype fuze components.
- Initiate the construction of prototype fuze circuits.
- Continue simulation effort.

5. PERSONNEL

During this reporting period, the following personnel worked on this program for the number of hours indicated.

Name	Program Function	Hours
A.J. Eisenberger	Program Manager	223
P. Kaszerman	System Engineer	168
R.F. De Mattos	Tester RF & Fuze	34
H.J. Curnan	Laser Trimmer & Fuze Microcircuits	56
G.L. Freed	Digitial Components	35
C.A. Zuroff	Programming	8
U.Z. Escoli	Mechanical Design	143
A.H. Owens	Mechanical Design	6
H. Wetteraur	Draftsman	137

APPENDIX A

M732 FUZE DESCRIPTION

A-1. INTRODUCTION

This appendix describes the progress, to date, in the construction of a mathematical model for the M732 fuze oscillator. The purpose of the model is to predict quantitatively the effect of adjusting certain trimming capacitors on those oscillator parameters that are of most interest. The model is constructed in terms of parameters, which are to be determined from a small number of very simple measurements made on the oscillators as they come off the production line. The sole criterion for the success of the model is its ability to predict correctly just which trimming capacitors must be added to bring a given unit within specification. This will enable the raw data to be fed into a computer, whose output will indicate which adjustments must be made. Thus, the need for costly and time-consuming trial-and-error modifications will be eliminated.

Paragraph A-2 of this appendix provides a discussion of the oscillator circuit, including the measurement results of a number of oscillators. These are the experimental results that the model must be able to explain. Paragraph A-3 provides a discussion of the *Linear Model* (LM). In the LM, the transistor is viewed as a two-port network characterized by four complex numbers (e.g., s-parameters). Although small signal s-parameter measurements were made on the transistors used in the experiment, it is not essential for the LM to be describable in terms of this small signal data. For the purposes of the LM, we allow the effective large-signal s-parameters to differ from the small signal values by an arbitrary amount. The essential feature of the LM is that the s-parameters be *constant* (i.e., independent of all voltage and current levels).

We will see shortly that, as a first approximation, the LM is indeed very good. It enables frequency and output power to be predicted very accurately (i.e., better than 1 percent). There is, however, another parameter that is of even greater interest than either the power or the frequency, and that is the *sensitivity* of the oscillator. This quantity is defined in paragraph A-3. It is shown that the sensitivity may be viewed as the difference between a dc voltage, which appears across a diode in the oscillator tank circuit when there is no reflected energy, and the corresponding dc voltage across this diode when such reflections are present. The LM is capable of predicting either dc voltage quite accurately (to within a few percent). However, when the two values are subtracted, the difference is quite small, and the error is large. It is here that the LM breaks down. Power, frequency, and voltage are *first-order* quantities, and here the LM does very well. However, sensitivity is a *second-order* quantity, and the LM is inadequate. In fact, in paragraph A-3 we show, with the help of a few simplifying assumptions, that no LM can predict the observed changes in sensitivity with trimming capacitance.

Therefore, in paragraph A-4, we refer to a Nonlinear Model (NLM). Although the results are not yet complete, preliminary indications seem to show that the NLM is quite successful. It retains the ability of the LM to predict frequency and power, and at the same time yields usable results for sensitivity as a function of trimming capacitances.

A-2. RF CIRCUIT AND EXPERIMENTAL RESULTS

For the purposes of this appendix, we assume the rf circuit to be as shown in Figure A-1. The transistor is in the common base configuration with no external load between emitter and base. Feedback is achieved via the internal emitter-to-base and emitter-to-collector capacitances, which are not shown. The tank circuit, which also doubles as an antenna, is represented by the branch through which current i' is shown to flow. The real part of the antenna impedance consists of a radiation resistance:[1]

$$Rr = 20\ W^4A^2/c^4 \text{ ohms}, \qquad (1)$$

together with an ohmic loss contribution Rs. In Equation 1, A is the area of the loop and c is the speed of light. The voltage v represents the effect of reflected energy. The reactive components consist of a fixed (distributed) inductance Lo, and a number of fixed capacitances lumped together under the designation Co. In addition, there is a capacitance C_1 whose value may be altered by adding a number of capacitive pads,[2] called the *series capacitor*. In addition, there is capacitance C_2, which is variable in the same manner, and which shunts the entire antenna assembly. This is called the *shunt capacitor*. It is the effect of the variation of these two capacitances on sensitivity that are the primary concern of this appendix.

We must now, therefore, define what we mean by sensitivity. In practice, the oscillator is placed in a small chamber with absorbing walls called a load chamber. A spinning disc, containing a strip of metal (or equivalent modulation), is placed overhead. The rms component of voltage that appears across the diode (shown in phantom in Figure A-1), due to the variation in reflections caused by the spinning disc, is measured and defined as the sensitivity.[3,4] It will readily be appreciated that the sensitivity could be measured differently. We could stop the spinning disc and measure the dc voltage that appears across the diode under two conditions: first with the reflector at right angles to the plane of the loop, and second with the reflector in the plane of the loop (see Figure A-2). The first condition is denoted *condition O* (CDNO); the superscript O describes the values of various quantities under this condition, and it clearly represents the case of minimum reflections. The second condition is *condition R* and represents the case of maximum reflections. In terms of the dc voltages measured across the diode under these conditions, the sensitivity as just defined becomes:

$$S_M = (V_{DC}^{(O)} - V_{DC}^{(R)}) / 2\sqrt{2 \text{ volts.}} \qquad (2)$$

It is clear from Equation 2 that the sensitivity is the difference between two first-order quantities (i.e., it is a second-order quantity).

The sensitivity, along with power and frequency, was measured for some 50 transistors in two housings, which were modified to allow for the replacement of transistors without soldering.[5] These parameters were measured as a function of C_1 and C_2. The salient features of these measurements are shown schematically in Figure A-3.

In all cases, dc voltage is found as a decreasing function of capacity. It is also found that for a given capacitance, the condition R voltage is less than the condition O voltage. However, as the parallel capacitance C_2 is increased, the two lines diverge, whereas when C_1 is increased, the two lines come together. In other words, the sensitivity is an *increasing* function of parallel capacitance, but a *decreasing* function of series capacitance.

The experimental results can be summarized as follows:

$$\text{a)} \quad V_{DC}^{(R)} < V_{DC}^{(O)} \text{ given } C_1 \text{ and } C_2,$$

$$\text{b)} \quad \frac{\partial V_{DC}^{(O)}}{\partial C_1} < \frac{\partial V_{DC}^{(R)}}{\partial C_1} < 0, \text{ and} \qquad (3)$$

$$\text{c)} \quad \frac{\partial V_{DC}^{(R)}}{\partial C_2} < \frac{\partial V_{DC}^{(O)}}{\partial C_2} < 0.$$

The paragraphs that follow provide a discussion of the LM. Under certain simplifying assumptions (that should nevertheless be quite accurate), we show that conditions (a), (b), and (c) above cannot be simultaneously satisfied.

A-3. THE LINEAR MODEL (LM)

In the LM, the transistor in Figure A-1 appears as a constant current source. This is most readily seen by representing the transistor as a two-port network in terms of Z-parameters (Z-parameters are more convenient to use in our case then the equivalent s-parameters). Since the emitter-base is open-circuited, we have (see Figure A-4):

$$I = -v_{eb}/z_{12} \quad , \tag{4}$$

where v_{eb} is the rf voltage appearing across the emitter-base. Of the four Z-parameters, only two enter into the equations. In addition to Z_{12} we have the *frequency condition:*[6]

$$Im(Z_{22} + Z_L) = 0. \tag{5}$$

A little care is required in writing Z_L because of the appearance of the impressed voltage v in the loop. Harrison[4] has derived an expression for the total loop impedance, including the effect of reflections, as seen by the transistor. As might have been anticipated, the effective voltage induced in the loop is seen to be proprotional to the antenna current i', and is used to write:

$$v = re^{j\phi} i' . \tag{6}$$

The value to be used for ϕ has not yet been entirely settled, the question being complicated by the fact that the dipole is in the *near field* of the antenna. If only far-field considerations were important, it could be argued that the radiative electric field from the loop excites a current in the dipole, which is in phase with the antenna current i'. An in-phase component of magnetic field travels back to the loop to induce an rf voltage that leads i' by 90^0, as follows:

$$\phi = -\pi/2 + 2\left(\frac{2\pi s}{\lambda}\right), \tag{7}$$

where s is the distance of the dipole from the loop. (This value appears to agree fairly well with the experiment). As a matter of fact, the NLM described in paragraph A-4 is almost entirely independent of Ø. This is because r and I are determined from the two dc voltage measurements, $V_{DC}^{(O)}$ and $V_{DC}^{(R)}$, made with no pads in, and the variation of I back-fitted from the measured values of V_{DC}. The phase drops out, except for the small variation in V_{cb} with Ø. However, it is important to note that conservation of energy implies that r cos Ø < Rr. Thus, it must be assured that a Ø exists such that for the assumed values of the other circuit parameters, this condition can be satisfied.

The circuit that has to be solved is shown in Figure A-5. The circuit equations are as follows:

$$\left\{(R-r\cos\phi) + j\left[\left(WL - \frac{1}{WC}\right) - r\sin\phi\right]\right\} i' = -\frac{j}{WC_2} i'' \tag{8}$$

where: i and I are related by:

$$I = i' + i''$$

and where:

$$R = Rs + Rr ,$$

$$\frac{1}{C} = \frac{1}{Co} + \frac{1}{C_1} , \text{ and}$$

$$L = Lo .$$

From Equation 8, we find that:

$$i' = \frac{-j}{WC_2} \quad \frac{I}{\left\{(R-r\cos\phi) + j\left[\left(WL - \frac{1}{\tilde{WC}}\right) - r\sin\phi\right]\right\}} \tag{9}$$

where: $\frac{1}{\tilde{C}} = \frac{1}{C_0} + \frac{1}{C_1} + \frac{1}{C_2}$.

Using Figure A-1, we can now write the expressions for $V_{DC}^{(O)}$ and $V_{DC}^{(R)}$. V_{DC}, in general, is the product of the absolute magnitude of the rf voltage across the diode times some efficiency factor η, which should be fairly close to unity. We find in fact that:

$$V_{DC}^{(R)} = \frac{\eta I}{\omega C_2} \left\{ \frac{(R + r\cos\phi)^2 + (\omega L - \frac{1}{\omega C_0} + r\sin\phi)^2}{(R - r\cos\phi)^2 + (\omega L - \frac{1}{\tilde{\omega} C} - r\sin\phi)^2} \right\}^{1/2}, \qquad (10A)$$

so that the corresponding equation for $V_{DC}^{(O)}$ is:

$$V_{DC}^{(O)} = \frac{\eta I}{\omega C_2} \left\{ \frac{R^2 + (\omega L - \frac{1}{\omega C_0})^2}{R^2 + (\omega L - \frac{1}{\tilde{\omega} C})^2} \right\}^{1/2} \qquad (10B)$$

Before analyzing Equations 10A and 10B, we consider the frequency and the power, which are predicted quite well by the LM.

Using Equation 8 we first have:

$$Z_L = v_{CB/I} = -\frac{j}{\omega C_2} \frac{i''}{I}$$

$$= -j \quad \frac{(R - r\cos\phi) + j(X - r\sin\phi)}{(R - r\cos\phi) + j(\tilde{X} - r\sin\phi)}, \qquad (11)$$

$$\omega C_2$$

where we introduce the following notation:

$$X = (\omega L - \frac{1}{\omega C}) \text{ and}$$

$$\tilde{X} = (\omega L - \frac{1}{\tilde{\omega} C}) \quad .$$

Using our superscript O and R convention, we can extend these definitions to read:

$$X^{(R)} = (\omega L - \frac{1}{\omega C}) - r\sin\phi \text{ and}$$

$$\tilde{X}^{(R)} = \left(WL - \frac{1}{\tilde{W}C}\right) - r \sin \phi.$$

Similarly, we write:

$$R^{(R)} = Rr + Rs - r \cos \phi.$$

Now the frequency condition in Equation 5 reads:

$$X_{22} - \frac{1}{WC_2} \left\{ \frac{R^{(R)\,2} + X^{(R)}\,\tilde{X}^{(R)}}{R^{(R)\,2} + \tilde{X}^{(R)\,2}} \right\} = 0. \tag{12}$$

This equation has been solved for W and the values obtained agree well with the experiment[6] (see Table A-1).

The theoretical power radiated is given by:

$$P_T^{(R)} = \frac{1}{2}\left|i'\right|^2 Rr$$

$$= \frac{1}{2} \frac{I^2 Rr}{W^2 C_2^{\,2}\left[(R - r\cos\phi)^2 + (WL - \frac{1}{\tilde{W}C} - r\sin\phi)^2\right]} \tag{13}$$

Actually, it is not possible to compare Equation 13 directly with the experiment for two reasons. First, we do not know the values of I and r, and second, only relative rather than absolute power measurements were obtainable from the load chamber that was available when the measurements were made. However, we can determine whether the predicted behavior with capacitance represents reality. We can determine I and r from measurements of $V_{DC}^{(R)}$ and $V_{DC}^{(O)}$ under the conditions of, say, minimum C_1 and C_2. Moreover, we can measure the relative power under these same conditions and assume that Equation 12 holds. Then we can see if the dependence on C_1 and C_2 predicted by Equation 12 corresponds with the experiment. Referring to Table A-2, it can be seen that the correspondence holds fairly well. (But the variations between $P_T^{(R)}$ and $P_T^{(O)}$ for given C_1 and C_2 should be ignored for two reasons. The first reason is that these are second-order variations and therefore not predicted very well by the LM. The second is for experimental reasons we will not go into here; these measured values are probably not very reliable anyway.)

Table A-1. Measured vs Computed Frequencies

S/N	Condition	Frequency	
		Measured	Calculated
1	A	43.11	45
	B	43.05	46
	C	36.8	35
	D	36.3	38
	E	38.0	36
	F	38.8	37
3	A	41.15	44
	B	40.9	45
	C	36.35	35
	D	35.9	36
	E	36.8	35
	F	35.4	36
4	A	41.1	44
	B	40.9	45
	C	35.6	35
	D	35.5	37
	E	36.8	35
	F	36.2	36
10	A	41.1	44
	B	40.9	45
	C	36.1	35
	D	35.6	36
	E	36.7	35
	F	36.5	36

* Leading digits suppressed.

Table A-1. Measured vs Computed Frequencies (Continued)

S/N	Condition	Frequency*	
		Measured	Calculated
22	A	45.0	45
	B	.44.9	45
	C	41.1	35
	D	40.8	37
	E	40.9	36
	F	41.0	37
26	A	44.93	45
	B	44.88	46
	C	41.0	35
	D	40.9	38
	E	40.63	37
	F	40.65	38
33	A	43.7	45
	B	43.5	46
	C	41.1	35
	D	41.0	38
	E	41.1	37
	F	41.0	38

* Leading digits suppressed.

Note: Frequencies were computed to two significant places. For the value of inductance chosen for this run, several transistors had no solutions within the frequency range of interest.

Table A-1. Measured vs Computed Frequencies (Continued)

KEY:

Condition		Capacitive Pads
A	O	None
B	R	
C	O	Parallel only
D	R	
E	O	Series only
F	R	

Table A-2. Calculated vs Measured Power (Normalized) Based On The LM

S/N	Power (mW)				
	No Pads	Parallel Pads		Series Pads	
	Measured	Measured	Calculated	Measured	Calculated
1	246	260	268	260	288
4	294	270	318	315	342
5	248	260	264	252	288
8	277	267	295	296	319
16	282	294	300	303	327

Note: Values are for $P_T^{(O)}$. The small variation between $P_T^{(O)}$ and $P_t^{(R)}$ are not predicted well by the LM.

It is not difficult to see that the LM is unable to reproduce all the inequalities listed in Equation 3. Thus, differentiating Equation 10A (neglecting changes in W) we find:

$$\frac{\partial V_{DC}^{(R)}}{\partial C_2} = -\left[\frac{1}{C_2} + \frac{(\tilde{x} - r \sin \phi)\ 1/WC_2^2}{(R - r \cos \phi)^2 + (\tilde{x} - r \sin \phi)^2}\right] V_{DC}^{(R)} \quad \text{and} \quad (14)$$

$$\frac{\partial V_{DC}^{(R)}}{\partial C_1} = \left[\frac{-(\tilde{x} - r \sin \phi)\ 1/WC_1^2}{(R - V \cos \phi)^2 + (\tilde{x} - r \sin \phi)^2}\right] V_{DC}^{(R)} \quad . \quad (15)$$

It is clear that $\tilde{x}$ must be negative or Equation 5 has no solutions (x_{22} is always found to be negative). Thus, for example, to satisfy:

$$\frac{\partial V_{DC}^{(R)}}{\partial C_1} < 0,$$

we must have r sin ϕ negative and larger in magnitude than x, which is an unreasonable requirement. Furthermore, even if Equation 3b is satisfied, we find that:

$$\left[\frac{|\tilde{x}|\ \frac{1}{WC_1}^2}{R^2 + \tilde{x}^2}\right] V_{DC}^{(O)} > \left[\frac{|\tilde{x} - r \sin \phi|\ \frac{1}{WC_1}^2}{(R - r \cos \phi)^2 + (\tilde{x} - r \sin \phi)^2}\right] V_{DC}^{(R)}$$

Inequality A

In addition, Equation 3C implies that:

$$\left[\frac{1}{C_2} + \frac{|(\tilde{x} - r \sin \phi)|\ \frac{1}{WC_2}^2}{(R - r \cos \phi)^2 + (\tilde{x} - \sin \phi)^2}\right] V_{DC}^{(R)} > \left[\frac{1}{C_2} + \frac{|\tilde{x}|^2/WC_2^2}{R^2 + \tilde{x}^2}\right] V_{DC}^{(O)}$$

or, since we found from Equation 3A that $V_{DC}^{(R)} \quad V_{DC}^{(O)}$, this last inequality implies that:

$$\left[\frac{|(\tilde{x} - r \sin \phi)| \frac{1}{WC_2}^2}{(R - r \cos \phi)^2 + (\tilde{x} - r \sin \phi)^2}\right] V_{DC}^{(R)} > \left[\frac{|x|/WC_2^2}{R^2 + \tilde{x}^2}\right] V_{DC}^{(O)}.$$

Inequality B

Clearly, inequalities A and B are contradictory, which shows that the LM is inconsistent with *all* of the inequalitites in Equation 3.

A-4. NONLINEAR MODEL (NLM): REMAINING PROBLEMS

Although the LM successfully predicts all first-order quantities (such as frequency, power, and voltage) to within a few percent or better, it cannot account for small differences between these quantities, i.e., it breaks down for second-order quantities (refer to paragraph A-3). It has been shown that sensitivity is a second-order quantity; thus, it is not surprising that the LM is unsuccessful in predicting sensitivity behavior as a function of changes in parallel and series capacitance.

Since sensitivity is the quantity of greatest interest in the oscillator analysis, we must go beyond a simple LM. However, when an NLM is considered, the problem is not as well-defined. Once the circuit in Figure A-1 is accepted as the correct one for the oscillator, and a linear parameterization of the transistor is required, then the LM becomes a well-defined mathematical problem. In other words, there is only one LM, but there are many NLMs.

Because of this, it was felt that an attempt to base an NLM on first principles might prove too time-consuming. Instead, it was decided to let the experimental data provide the structure of the model in a manner explained in the paragraphs that follow. The usefulness of the model depends upon its ability to predict. In this respect, preliminary results indicate that it is quite useful as a calculation tool, even though the physics on which it is based is not entirely clear.

The most likely point at which the LM breaks down is the quantity I in Equation 4; it seems fairly clear that in actuality I is not a constant, but depends upon the collector - base voltage v_{cb}. A program was run on the Burroughs 6700 to determine, from experimental data, the functional dependence of I on v_{cb}. The inputs used were power, frequency, and detector voltage data, under conditions O and R, as a function of parallel and series capacitances for 40 motorola transistors and several RCA transistors.

The results show that in almost all cases the points fall very close to a single curve, whose nature is shown schematically in Figure A-6. The general shape of the curve is quite reasonable. I is approximately constant for small v_{cb}, and falls off as v_{cb} becomes large. The rise at intermediate v_{cb}'s might also have been predicted; it is necessary in order to explain the increase in sensitivity as C_2 is increased. In general, it is very difficult to explain, on the basis of the LM alone, how increasing the parallel capacitance can increase the sensitivity.

The NLM, then, is a model that satisfies all the equations of the LM except that I, and instead of being a constant, is allowed to vary in the manner indicated in Figure A-6.

First, the curve in Figure A-6 was approximated by the 3-level, piece-wise continuous function of Figure A-7, and sensitivities were calculated on the computer. Some early measurements were taken in two different, uncalibrated load chambers. A different back-fit was used in each case. In all cases, the I vs v_{cb} curves were essentially in the same form as shown in Figure A-7, but the levels and break-points had to be shifted. It is believed that the effects on different (uncalibrated) load chambers is to change the details of the I vs v_{cb} curves, but to leave the general character of the model the same. This point, however, needs more thorough testing.

Another problem with these early measurements is that the curves were insufficiently accurate and suffered from repeatability problems. Although it was not fully recognized at the time, dc voltage readings with the reflector in either the O or R position take many minutes to stabilize. If insufficient stabilization time is allowed, erroneous sensitivity values result. This drift in dc voltage with time is not felt to be a problem, since it is believed that the O and R condition voltages drift together. Thus, the sensitivity stabilizes rather quickly (in seconds) even though the dc voltages continue to drift. This is another matter that requires further substantiation.

More careful measurements were taken at a later date, and the results of theory vs experiment for these more recent results are shown in Table A-3. In this case theory and experiment are in much closer agreement. Thus far, measurements have been repeated only on a group of low f_T motorola transistors. It is planned to extend these measurements to other groups of transistors in the near future.

In conclusion, it can be said that our NLM seems capable of predicting all the quantities of interest quite well, including sensitivity. However, before the value of the NLM can be considered firmly established, the three unfinished tasks mentioned previously must be completed.

Table A-3. Calculated vs Measured Values of Sensitivity Based on Recent Data for the NLM

	No Pads	Parallel Pads		Series Pads	
S/N	Measured (mV)	Measured (mV)	Calculated (mV)	Measured (mV)	Calculated (mV)
θ = 0 degrees					
1	.197	.339	.339	.158	.158
4	.245	.406	.415	.184	.183
5	.195	.322	.312	.152	.148
8	.222	.360	.371	.152	.161
16	.217	.369	.344	.151	.159
θ = 90 degrees					
1	.197	.339	.339	.158	.158
4	.245	.406	.416	.184	.180
5	.195	.322	.316	.152	.147
8	.222	.360	.384	.152	.159
16	.217	.369	.355	.151	.159

Note: The nonlinear curve was fitted to SN1 exactly.

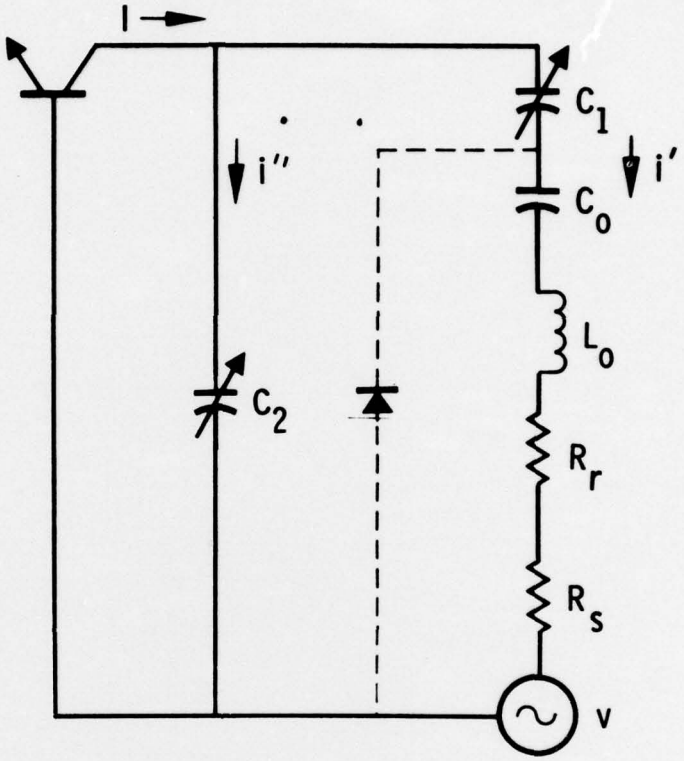
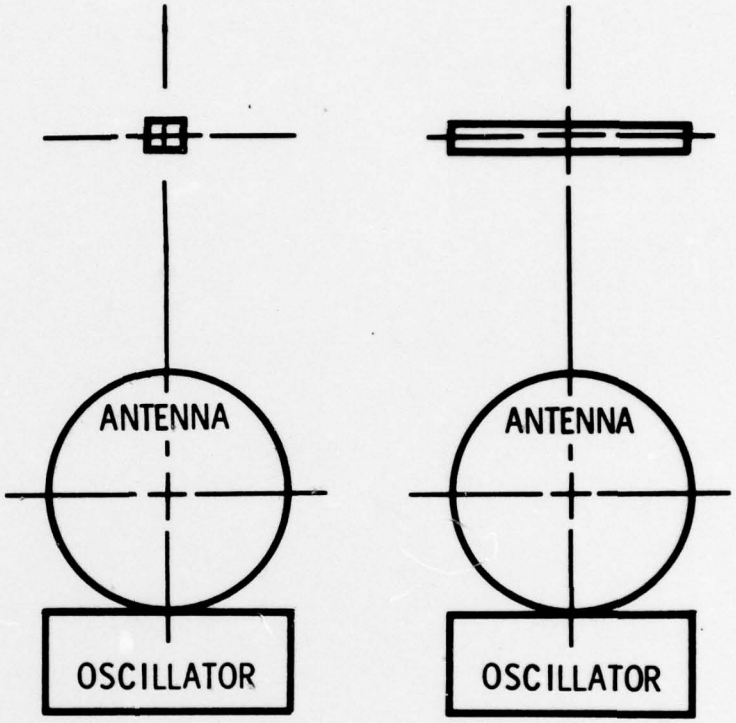


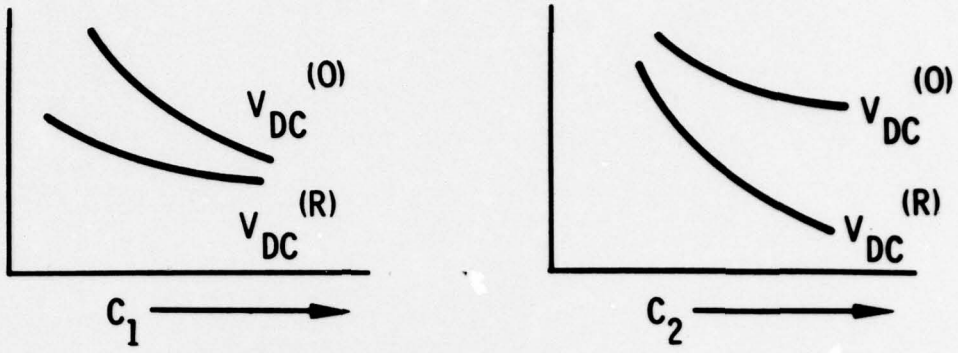
Figure A-1. Rf Circuit of the M732 Fuze Oscillator



CONDITION O: DIPOLE AT RIGHT ANGLES TO PLANE OF THE LOOP (MINIMUM REFLECTIONS)

CONDITION R: DIPOLE IN THE PLANE OF THE LOOP (MAXIMUM REFLECTIONS)

Figure A-2. Static Measurement of Sensitivity



NOTE:

$V_{dc}^{(O)}$ IS THE dc VOLTAGE UNDER CONDITION O;

$V_{dc}^{(R)}$ IS THE dc VOLTAGE UNDER CONDITION R (SEE FIG. A-2)

Figure A-3. Dc Voltage vs Capacitance

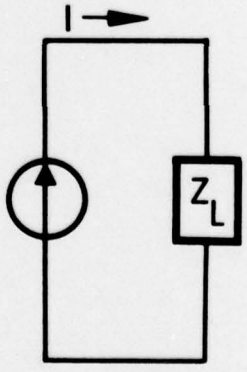


Figure A-4. Equivalent Circuit for the Linear Analysis

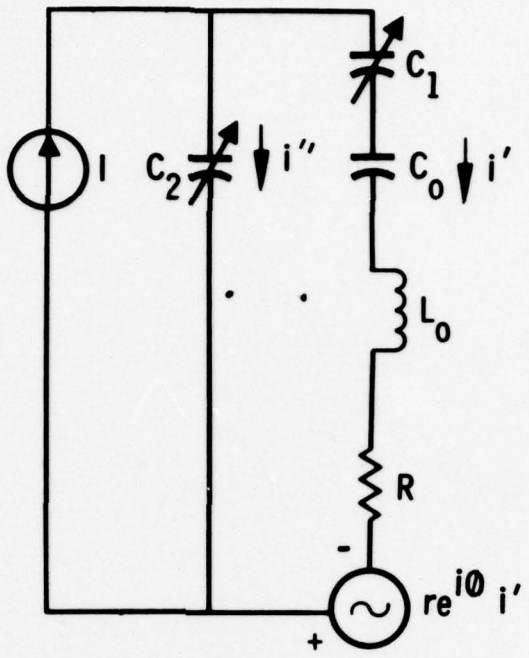


Figure A-5. Detailed Circuit for the LM

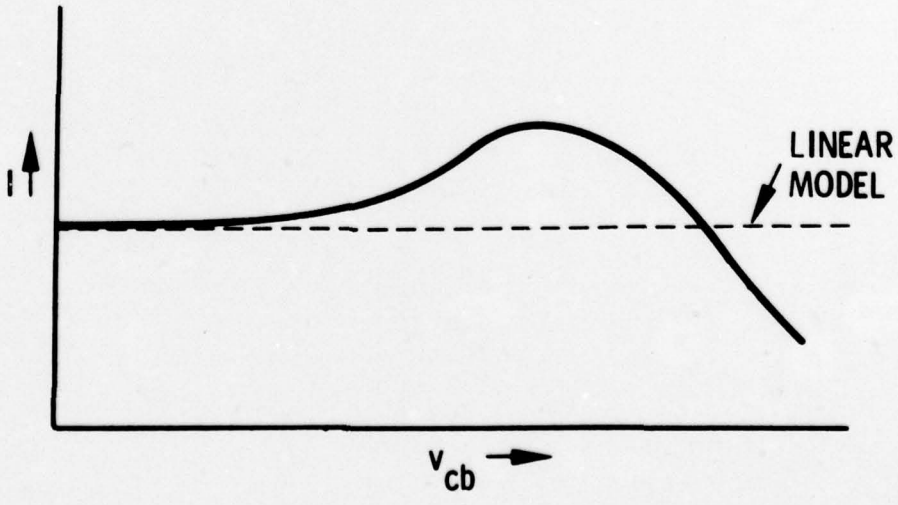


Figure A-6. I as a Function of V_{cb}

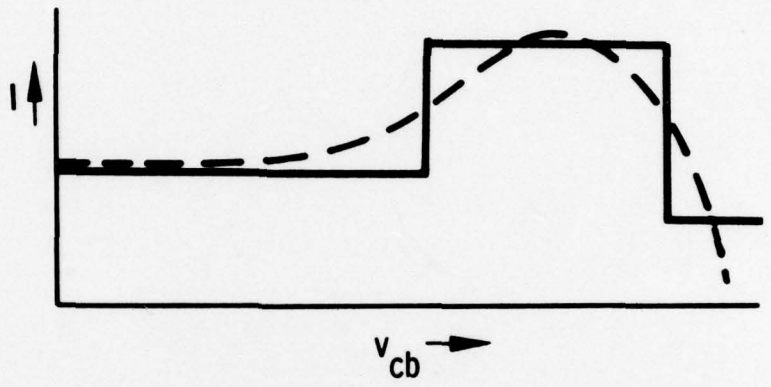


Figure A-7. Approximation of $I(v_{cb})$ by a 3-Level Step Function

REFERENCES

(1) See for example: S. Ramo and J.R. Whinnery, "Fields and Waves in Modern Radio," 2nd Edition, Wiley & Sons, NY (1953), Chapter 12.

(2) The physical configuration of the oscillator is described by Section 2-2 and Figure A-2, First Quarterly Report.

(3) The reason sensitivity is important, and the relationship between the sensitivity discussed in this report and the *true* sensitivity under field conditions, is discussed elsewhere. See for example: E. Harrison, "Load Box Measurement of Loop Fuze Oscillator Sensitivity and Radiated Power (U)," Harry Diamond Laboratories, HDL-TR-1594, April 1972 (SECRET).

(4) A careful mathematical analysis of the load chamber has been done by E. Harrison, "Load Box Measurement of Loop Fuze Oscillator Sensitivity and Radiated Power (U)," Harry Diamond Laboratories, HDL-TR-1594, April 1972 (SECRET).

(5) Measurements were taken at LEC by R.F. DeMattos and J. Gillespie.

(6) As mentioned earlier, the frequency of oscillation, including the effects of changing C_1 and C_2, are predicted quite accurately by the LM (See Table A-1). The values of Z_{22} were computed from the measured values of small signal s-parameters. However, the small changes involved in going from condition O to condition R, with C_1 and C_2 fixed, represent a second-order perturbation and are not always reproduced as well. It should also be noted that when in solving for frequency, in Equation 5, generally *two* roots are found in the frequency range of interest. Table A-1 lists the lower

of these two roots. We surmise that the upper value is excluded by the condition on the sign of the real part of the *starting* condition ($Z_{22} + Z_L$), but this assumption needs to be tested.

See for example: Communications Handbook, Part II. Edited by J.R. Miller. Texas Instruments Inc. Dallas, Texas (1965), Chapter 3.

APPENDIX B
TRIMMABLE UNITS

TRIMMABLE CAPACITOR (OSCILLATOR SENSITIVITY ADJUSTMENT)

Capacitance measurements of the *preliminary* design were made on chips with leads at 1 MHz. The design goal of 2.0 picofarads, with equal 0.5-picofarad increments, was not achieved. Values closer to 3.0 picofarads, with increments in the range of 0.4 to 0.8 picofarads, were measured. There was a 0.65-picofarad residual fringing capacitance after all links were cut with a diamond scribing tool, and the leads contributed another 1.2 picofarads.

A new design is in progress to reduce fringing, centralize the starting point, *and* provide a 1, 2, or 4 incremental ratio. A high-density, small-particle size alumina substrate (MRC *SUPERSTRATE*) will be used to improve the consistency of the results (dielectric constant = 9.2 $\pm$ 3.5 percent). Redesigning the antenna is in progress with special attention being given to accurately positioning the capacitor chip so that hunting for the start point can be minimized.

TRIMMABLE RESISTOR (AMPLIFIER GAIN ADJUSTMENT)

The thick-film resistor chip design was completed (see Figure B-1). Some features incorporated are as follows:

- *Start Point Locators.* - The intersection of two orthogonal 5-mil lines, coprinted with the resistor paste, defines a point 20 mils from the edge of the resistor body and 20 mils from the termination conductor.
- *Alignment Marks.* - Alignment marks are provided at the diagonal extremes of the overall pattern to assure proper registering of the resistor pattern to the conductor. The

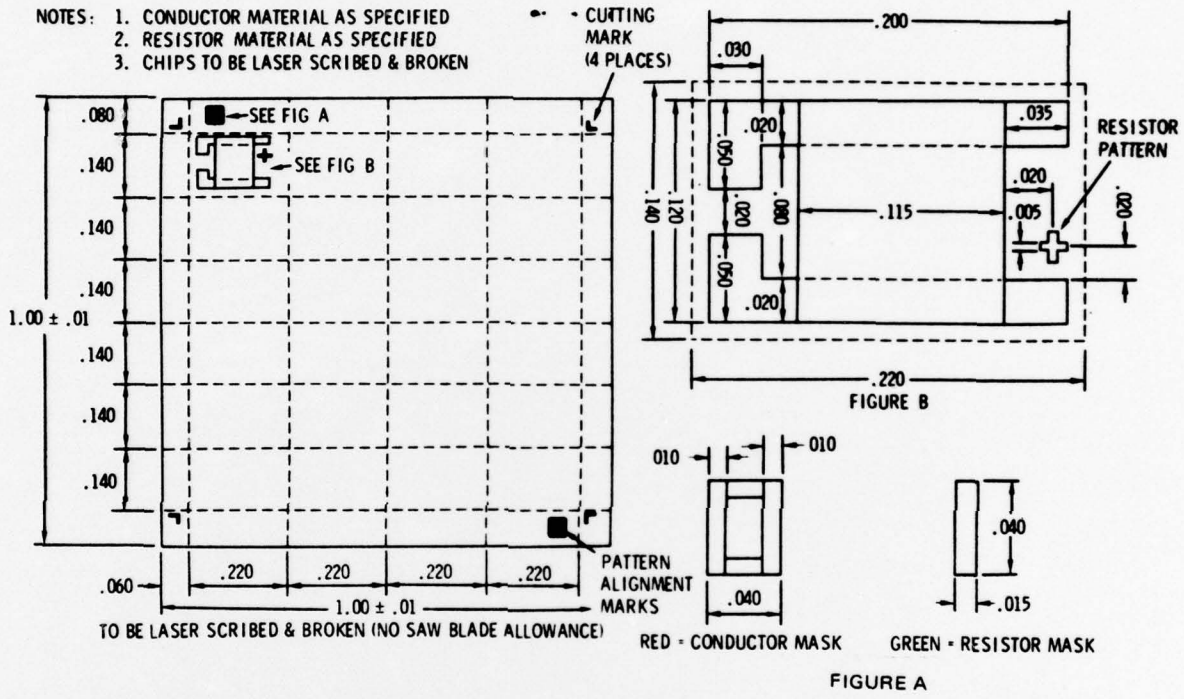


Figure B-1. Location of Multiple Patterns on Substrate

resistor body is also extended to the long edge of the termination pads as a further assistance.

- *Cutting Marks.* - *L*-shaped marks are coprinted with the conductor pattern to provide reference points for laser scribing the array of patterns into discrete chips. The patterns are screened in a 4 x 6 matrix on a 1-inch square substrate to obtain tight thickness distribution; thus, consistent laser-trimming results can be obtained.

Preliminary testing of seven different vendors' 1,000-ohm/square resistor paste has begun. As-fired resistance values, varying from 400 to 1,000 ohm (depending on vendor termination material and firing parameters), were obtained. The resistance distribution within any one substrate is quite good. It has been decided to mount the chip on the reverse side of the amplifier board, as a secondary operation. This will enable the test points to be probed from the same side of the board as laser-beam impingement takes place. This simplifies the mounting of the board into the workholder nest on the shuttle-feed mechanism.

Appendix C
Transient Response of Filter 1

The response of filter 1 (see Figure 13) to a carrier modulated step is found by using Laplace transforms. The Laplace transform of the carrier modulated step is:

$$\mathcal{L}[u(t)\cos wt] = \frac{s}{s^2 + w^2},$$

where: u(t) = unit step.

In the first quarterly report, the transfer function of the filter was shown as:

$$F(s) = \frac{A}{s-p_1} + \frac{B}{s-p_2} . \qquad (2)$$

The Laplace transform of the output of the filter is:

$$\mathcal{L}[\text{Output}] = \left[\frac{A}{s-p_1} + \frac{B}{s-p_2}\right]\left[\frac{s}{s^2 + w^2}\right]. \qquad (3)$$

Using Laplace transform tables gives the output response as:

$$f(t) = \frac{A}{p_1^2 + w^2}\left\{P_1\exp(P_1 t) + P_1^2 + w^2)^{1/2}\cos(wt + \theta_1)\right\}$$

$$+ \frac{B}{p_2^2 + w^2}\left\{P_2\exp(p_2 t) + P_2^2 + w^2)^{1/2}\cos(wt + \theta_2)\right\}, \qquad (4)$$

where:

p_1 = -1,469 radians/second,

p_2 = -24,133 radians/second,

$A = -1{,}379$ volts,

$B = 22{,}656$ volts,

$C = 0.94$ volts,

$D = -0.9$ volts,

$W = 2\pi f$,

$\theta_1 = \arctan \frac{w}{-p_1}$ and

$\theta_2 = \arctan \frac{w}{-p_2}$.

The transient portion of the response is:

$$\text{Transient} = A \frac{p_1}{p_1^2 + w^2} \ell^{p_1 t} + B \frac{p_2}{p_2^2 + w^2} \ell^{p_2 t} . \qquad (5)$$

The time constants of the terms in Equation 5 are $-1/p_1$ and $-1/p_2$, respectively. Using the values for p_1 and p_2 derived in the First Quarterly Report, the time constants are:

$$\gamma_1 = \frac{1}{1{,}149} \text{ second and}$$

$$\gamma_2 = \frac{1}{24{,}133} \text{ second.}$$

It is immediately seen that γ_2 is much less than a half-cycle and γ_1 is on the order of a half-cycle. However, the effect on the total transient is much less than that of γ_1, since the value of A in Equation 5 is less than 1/16 of the value of B. Thus, the transient can certainly be considered as completed in less than a cycle.

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Computer Test
Functional Test

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Work has been started to develop a dynamic test and correction system for electronic assemblies, capable of high speed operation. The system will be verified by testing and trimming 6000 M732 fuze components. A third generation test station has been designed. It will include a laser trimmer. Analysis of the fuze components and the test stimuli has been completed. A simulation of the entire system has been initiated. All electrical components for the fuze assemblies have been released.

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